



Department of Computer Applications
National Institute of Technology, Tiruchirappalli

1. Course Outline			
Course Title	Computer Organization and Architecture		
Course Code	CA715		
Department	CA	No. of Credits	3
Programme	MCA	Learning Hours	3
Course Type	Programme Core	Course Teacher	Dr. Mrs. B. Janet
Pre-requisites	Digital Computer Fundamentals		
E-mail	janet@nitt.edu	Telephone No.	0431-2503741
Course Type	Core Course	Office	Lyceum 108
Course moodle site	http://egov.nitt.edu/moodle/course/view.php?id=26		

2. Course Content
The Computer Organization and Architecture course deals with the study of data representation in computers and its internal circuits. It also explains the internal components of computer like CPU, Memory and I/O Devices and their characteristics. Various modern processor architecture will be evaluated.
3. Course Objectives
<ol style="list-style-type: none">1. To understand the data representation in a digital computer and explain how operations are performed by computer circuits2. To study and analyze the internal components of a computer and evaluate the performance of CPU, memory and I/O operations3. Study and analyze the modern processor architecture
4. Course Learning Outcomes (CO)
<ol style="list-style-type: none">1. Define binary number system and arithmetic operations. Design Boolean circuit for a given problem2. Analyze the different types of memory and their organization3. Describe the functional units of the CPU and its organization4. Discover the working and organization of I/O Devices5. Evaluate the different modern processor architecture.

5. Course Outcome (CO)	Aligned Programme Outcome (PO)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
Define binary number system and arithmetic operations. Design a Boolean circuit for a given problem	H	H	A	M	H	A	A	A	L	L	A	L
Analyze the different types of memory and their organization	H	H	A	M	H	A	A	A	L	L	A	L
Describe the functional units of the CPU and its organization	H	H	A	A	H	A	A	L	L	L	A	A
Discover the working and organization of I/O Devices	H	H	A	A	H	A	L	L	L	L	A	A
Evaluate the different modern processor architecture.	H	A	H	A	A	A	H	H	L	A	H	H

Lectures

Class lectures and class exercise with self-learning videos will form the primary teaching activity, the schedule for which is outlined below. Lecture material will address the intended learning objectives, and loosely follow the readings as specified in the Moodle course site. The lecture material will be made available before the class. The lectures are meant to be interactive, where learning takes place through interactive discussion in class. The Moodle site will be available for detailed content dissemination and discussion inside and outside the classroom, between students and with the teacher. Student engagement in class and in the Moodle online forum will count towards assessment of student participation that has 10% of assessment weightage.

Guest Lectures

Structured lectures will be supplemented by guest lectures by practitioners and researchers from industry and academia. These will serve to show the practical relevance of the course content and also expose the students to the open problems for research.

6. Course Teaching and Learning Activities

Week	Mode of Delivery	Topics	Readings
1.	Classroom activity	Introduction and Binary Number System	Refer Moodle Course Site
		Binary Arithmetic	
		Boolean Algebra	
2.	Classroom activity	Map Simplifications	
		Gates	
3.	Classroom activity	Combinational Circuits	
		Sequential Circuits	
		Memory: Internal	
4.	Classroom activity	External	
		Memory Organization	
		Associative Cache Virtual memory	
5.	Classroom activity	CPU: Arithmetic And Logic Unit	
		Instruction Sets	
		RISC - CISC	
6.	Classroom activity	Instruction pipeline	
		Addressing modes and formats	
		Register organization	
7.	Classroom activity	Control Unit Operation	
		Processor organization	
		External Devices: I/O modules	
8.	Classroom activity	Programmed I/O	
		Interrupt Driven I/O	
		Direct Memory Access	
9.	Classroom activity	I/O Channels	
		Asynchronous Data Transfer	
		Processors: Parallel	
10.	Classroom activity	Multi-core	
		Mobile	
		Embedded and Cloud computing/ IOT	

- All relevant material will be available in the course moodle site. Classroom activity includes lectures, tutorials, quiz, simulation exercise, laboratory exercise, mini-project, group task and seminar.

The assessment details for this course are given below. The assessment will be done for a total of 100 marks.

7. Course Assessment Methods – Theory					
Sl. No.	Mode of Assessment	Portions	Schedule	Duration in Minutes	Weightage (%)
1.	Test – 1	Unit I,II	4 th week	60	20
2.	Test – 2	Unit III,IV,V	8 th week	60	20
3.	Class activity	Periodic	Course duration	30	5
4.	Student participation	All Units	*	*	5
5.	End Semester Exam	All Units	November	120	50
Total					100

* Evaluated based on participation in lecture, class activity and moodle forum.

8. Essential Learning material (Textbooks, Reference books, Websites, Journals, etc.)
<ol style="list-style-type: none"> 1. William Stallings, “Computer Organization and Architecture”, 7th Edition, 2006, PHI. 2. M. Morris Mano and Michael D. Ciletti, “Digital Design”, 4th Edition, 2007, Pearson Education. 3. Hennessy J. and Patterson D., “Computer Architecture – A Quantitative Approach”, 1990, Morgan Kaufmann.
9. Course Exit Survey
<ul style="list-style-type: none"> • The students may give their feedback at any time to the course teacher or through a message in moodle which will be duly addressed. • The students may also give their feedback during Class Committee meeting and fill up the feedback form in moodle site at the end of each test.
10. Course Policy (including plagiarism, academic honesty, attendance, etc.)
<p>Classroom Behavior</p> <ul style="list-style-type: none"> • Ensure that the course atmosphere, both in the class, outside and on the online forum, is conducive for learning. Participate in discussions but do not dominate or be abusive. Be considerate of your fellow students and avoid disruptive behavior. <p>Exam policy</p> <ul style="list-style-type: none"> • Each student is required to take all exams at the scheduled times. All exceptions must be cleared with the professor prior to the exam time. Exams missed for insufficient reason and without being cleared with the professor prior to the exam time will be assigned a score of zero. <p>Assignments</p> <ul style="list-style-type: none"> • All assignments are due on or before the mentioned date and time and is to be uploaded on the course moodle site.

Late assignments

- Late submissions are not accepted.

Plagiarism

- The students are expected to come out with their original work on term activity, assignments and tests/examinations. If found to be plagiarized, it will be assigned a score of zero.

Attendance

- Attendance is expected. If a student misses a class, the student is still responsible for the material that is studied and for completing any assignments by the due date that may have been handed out by the instructor during class.

Academic Honesty

- i) No type of academic dishonesty will be tolerated. If the student is caught cheating (on the assignments, exams, or project) the punishment will be the most severe penalty allowed by the Institute policy.
- ii) Possession of any electronic device, if any, found during the test or exam, the student will be debarred for 3 years from appearing for the exam and this will be printed in the Grade statement/Transcript.
- iii) Tampering of MIS records, if any, found, then the results of the student will be withheld and the student will not be allowed to appear for the Placement interviews conducted by the Office of Training & Placement, besides (i).

11. Additional Course Information

- The students can get their doubts clarified during class.
- Prior request for appointment through mail, stating the subject matter to be discussed, is required to fix a time for discussion of subject matter outside class. Appointment time will be communicated through reply mail.

For Senate's Consideration

(Dr. Mrs B. Janet)

Course Faculty



(Dr. V. Gayathri)

PAC Chairperson



(Dr. A. Vadivel)

HoD