DEPARTMENT OF INSTRUMENTATION AND CONTROL ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	B.Tech- Instrumentation and Control Engineering		
Course Title	Digital Electronics		
Course Code	ICPC14	No. of Credits	3
Course Code of Pre-requisite subject(s)	NIL		
Session	July 2023	Section (if, applicable)	B
Name of Faculty	Dr .V Sridevi	Department	ICE
Email	sridevi@nitt.edu	Telephone No.	04312503361
Name of Course Coordinator(s) (if, applicable)	NA		
E-mail	NA	Telephone No.	NA
Course Type	■ Core course	☐ Elective course	

Syllabus (approved in BoS)

Review of number systems and logic gates, Algebraic reductions, Binary codes -Weighted and non-weighted, number complements, Binary arithmetic, Error detecting and error correcting codes, SOP, POS Canonical logic forms, Karnaugh maps and Quine-McClusky methods, Don't care conditions, minimization of multiple output functions.

Synthesis of combinational functions: Arithmetic circuits-Adder/ Subtractor, carry look-ahead adder, signed number addition and subtraction, BCD adders. IC adders. Multiplexers, implementation of combinational functions using multiplexers, de-multiplexers, decoders, code converters, Digital ICs for combinational logic circuits.

Sequential Logic: Basic latch circuit, Debouncing of a switch, Flip-Flops: truth table and excitation table, conversion of Flip-flops, integrated circuit flip-flops. Race in sequential circuits, Shift Registers, Counters - Synchronous, Asynchronous, Up-Down, Design of counters.

Analysis of clocked sequential circuits, Design with state equations, Moore and Mealy graphs, State reduction and assignment, Sequence detection, Hazards. Complexity and propagation delay analysis of circuits. Programmable logic devices, Design using Programmable Logic Devices (PLA, PAL, CPLD and FPGA).

Digital Hardware: Logic levels, Realization of logic gates, different logic families (TTL, ECL, CMOS, HC, HCT, ACT and HSCMOS), Logic levels, voltages and currents, fan-in, fan-out, speed, power dissipation. Comparison of logic families, interfacing between different families.

COURSE OBJECTIVES

The subject aims to provide the student with

1. An understanding of number systems, codes and their conversions.
2. The capability to reduce Boolean expression using K-map and tabular methods.
3. The ability to design and analyze combinational and sequential logic circuits for a given problem statement.
4. An understanding of digital hardware, different types of logic families and their characteristics

COURSE OUTCOMES (CO)

On completion of this course, the students will be able to,

1. Understand various number systems, conversions and simplify the logical expressions using Boolean functions
2. Design and develop arithmetic and other special functions using combinational logic circuits and PLDs.
3. Design and develop synchronous and asynchronous for the given problem statement.
4. Understand how logic gates are built from the fundamental semiconductor electronics and be able to select logic ICs from different families based on requirement.

Course Outcomes	Aligned Programme Outcomes (PO)
1. Understand various number systems, conversions and simplify the logical expressions using Boolean functions	1,2,12
2. Design and develop arithmetic and other special functions using combinational logic circuits and PLDs.	1,2,12
3. Design and develop synchronous and asynchronous for the given problem statement.	1,2,12
4. Understand how logic gates are built from the fundamental semiconductor electronics and be able to select logic ICs from different families based on requirement.	1,2,12

COURSE PLAN – PART II

COURSE OVERVIEW

This course covers combinational and sequential logic circuits. Topics include number systems, Boolean algebra, logic families, medium scale integration (MSI) and large-scale integration (LSI) circuits, analysis and design of combinational and sequential circuits. Upon completion, students should be able to construct, analyze, verify, and troubleshoot digital circuits using appropriate techniques and test equipment

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1	1st& 2nd Week	Review of number systems and logic gates, Algebraic reductions, Binary codes -Weighted and non-weighted, number compliments, Binary arithmetic, Error detecting and error correcting codes	Chalk and Talk

2	3rd& 4th week	SOP, POS Canonical logic forms, Karnaugh maps and Quine-McClusky methods, Don't care conditions, minimization of multiple output functions. Synthesis of combinational functions: Arithmetic circuits-Adder/Subtractor, carry look-ahead adder, signed number addition and subtraction, BCD adders. IC adders.	Chalk and Talk
3	5th& 6th week	Multiplexers, implementation of combinational functions using multiplexers, de-multiplexers, decoders, code converters, Digital ICs for combinational logic circuits, Complexity and propagation delay analysis of circuits.	Chalk and Talk
TEST 1			
4	7th& 8th week	Sequential Logic: Basic latch circuit, Debouncing of a switch, Flip-Flops: truth table and excitation table, conversion of Flip-flops, integrated circuit flip-flops. Race in sequential circuits,.	Chalk and Talk
5	9th& 10th week	Shift Registers, Counters - Synchronous, Asynchronous, Up-Down, Design of counters Analysis of clocked sequential circuits.	Chalk and Talk
6	11th& 12th week	Design with state equations, Moore and Mealy graphs, State reduction and assignment, Sequence detection, Hazards. Programmable logic devices, Design using Programmable Logic Devices (ROM, PLA, FPGA).	Chalk and Talk
TEST 2			
7	13th& 14th week	Digital Hardware: Logic levels, Digital integrated circuits, Logic delay times, Fan-Out and Fan-In, Logic families, Interfacing between different families. CMOS Electronics: CMOS electronics and Electronic logic gates, The CMOS inverter, Logic formation using MOSFETs, CMOS memories.	Chalk and Talk

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Written Test 1	1st week of September	1 Hour	15
2	Written Test 2	2nd week of October	1 Hour	20
CPA	Compensation Assessment*	3rd week of November	1 Hour	15/20
3	Assignment/Programming Assisgnment	--	--	25
4	Final Assessment	2nd week of December	3 Hours	40

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

1. Anonymous feedback through questionnaire.
2. Feedback from the students during the class committee meetings.

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

MODE OF CORRESPONDENCE (email/ phone etc) - Email & Phone

COMPENSATION ASSESSMENT POLICY

Compensation test will be conducted for students who miss Test1 or Test2 (only written test). But they should get permission from the faculty by giving valid reason in written form to write retest.

Grading Policy

The students will be graded relatively with all the four assessment marks put together with the passing minimum shall be 35% or Class Average/2, whichever is maximum. Those who have obtained F grade should appear for supplementary examination, that will be conducted during the first week of next semester. If the student get F grade in the supplementary examination will have to reappear till the student passes the course.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

It is mandatory to maintain 75% attendance to appear for end semester examination. The students having less than 75% of attendance will not be allowed to write the end semester examination. The student he/she having less than 75% of attendance has to redo the course in the forth coming semester.

ACADEMIC DISHONESTY & PLAGIARISM

Academic honesty:

The students have the freedom to do their work meanwhile; they have to obey the institute academic rules. The students will not be involved plagiarizing other student's assignment work, peer's examination answer sheet and any mode of copying other's work.
The students involved in these activities are penalized and their name list will be sent to the office of Dean (Academic) for legal action.

ADDITIONAL INFORMATION - NIL

FOR APPROVAL

Course Faculty _____ (Dr V Sridevi) CC-Chairperson _____ HOD _____