NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

DEPARTMENT OF ICE

COURSE PLAN – PART I			
Name of the programme and specialization	B.Tech		
Course Title	Digital Electronics		
Course Code	ICPC14	No. of Credits	3
Course Code of Pre-requisite subject(s)	NIL		
Session	July 2023	Section (if, applicable)	A
Name of Faculty	Dr. D. Ezhilarasi	Department	ICE
Official Email	ezhil@nitt.edu	Telephone No.	9444878908
Name of Course Coordinator(s) (if, applicable)	NA		
Official E-mail	NA	Telephone No.	NA
Course Type (please tick appropriately)	☑ Core course	☐ Elective course	

Syllabus (approved in BoS)

Review of numbersystems and logic gates, Algebraic reductions, Binary codes -Weighted and non-weighted, number complements, Binary arithmetic, Error detecting and error correcting codes, SOP, POS Canonical logic forms, Karnaugh maps and Quine-McClusky methods, Don't care conditions, minimization of multiple output functions.

Synthesis of combinational functions: Arithmetic Circuits-Adder/ Subtractor, carry look-ahead adder, signed number addition and subtraction, BCD adders. IC adders. Multiplexers, implementation of combinational functions using multiplexers, de-multiplexers, decoders, code converters, Digital ICs for combinational logic circuits.

Sequential Logic: Basic latch circuit, Debouncing of a switch, Flip-Flops: truth table and excitation table, conversion of Flip-flops, integrated circuit flip-flops. Race in sequential circuits, Shift Registers, Counters - Synchronous, Asynchronous, Up-Down, Design of counters.

Analysis of clocked sequential circuits, Design with state equations, Moore and Mealy graphs, State reduction and assignment, Sequence detection, Hazards. Complexity and propagation delay analysis of circuits. Programmable logic devices, Design using Programmable Logic Devices (PLA, PAL, CPLD and FPGA).

Digital Hardware: Logic levels, Realization of logic gates, different logic families (TTL, ECL, CMOS, HC, HCT, ACT and HSCMOS), Logic levels, voltages and currents, fan-in, fan-out, speed, power dissipation. Comparison of logic families, interfacing between different families.

Reference Books:

1. M. Morris Mano, Charles Kime , Tom Martin, Logic and Computer Design Fundamentals ,Pearson, 5thEdition, 2016

2. Anil K Maini, "Digital Electronics: Principles and Integrated Circuits", Wiley, 2019
3. W. H. Gothmann, "Digital Electronics - An Introduction to Theory and Practice", Prentice Hall of India, 2000
4. Thomas L. Floyd, "Digital Fundamentals", 11th Edition, Pearson, 2015
5. Ronald J. Tocci, Widmer Neal, Moss Greg, "Digital Systems- Principles and Applications",12th Edition, Prentice Hall, 2010
5. J.M. Rabaey, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Prentice Hall of India, 2003

COURSE OBJECTIVES

The subject aims to provide the student with
1. An understanding of number systems, codes and their conversions.
2. The capability to reduce Boolean expression using K-map and tabular methods.
3. The ability to design and analyze combinational and sequential logic circuits for a given problem statement.
4. An understanding of digital hardware, different types of logic families and their characteristics

MAPPING OF COs with POs

Course Outcomes On completion of this course, the students will be able to	Programme Outcomes (PO) (Enter Numbers only)
1. Understand various number systems, conversions and simplify the logical expressions using Boolean functions	1,2,12
2. Design and develop arithmetic and other special functions using combinational logic circuits and PLDs	1,2,12
3. Design and develop synchronous and asynchronous circuits for the given problem statement	1,2,12
4. Understand how logic gates are built from the fundamental semiconductor electronics and be able to select logic ICs from different families based on requirement	1,2,12

COURSE PLAN – PART II

COURSE OVERVIEW

This course covers combinational and sequential logic circuits. Topics include number systems, Boolean algebra, logic families, medium scale integration (MSI) and large scale integration (LSI) circuits, analysis and design of combinational and sequential circuits. Upon completion, students should be able to construct, analyze, verify, and troubleshoot digital circuits using appropriate techniques and test equipment.

COURSE TEACHING AND LEARNING ACTIVITIES (Add more rows)

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1	1st & 2nd Week	Review of number systems and logic gates, Algebraic reductions, Binary codes -Weighted and non-weighted, number compliments, Binary	Chalk and Talk

		arithmetic, Error detecting and error correcting codes	
2	3rd & 4th week	SOP, POS, Canonical logic forms, Karnaugh maps, Don't care conditions, minimization of multiple output functions. Synthesis of combinational functions: Arithmetic circuits-Adder/Subtractor, carry look-ahead adder, signed number addition and subtraction, BCD adders. IC adders.	Chalk and Talk
3	5th & 6th week	Multiplexers, implementation of combinational functions using multiplexers, de-multiplexers, decoders, code converters, Digital ICs for combinational logic circuits, Complexity and propagation delay analysis of circuits.	Chalk and Talk
4	7th & 8th week	Sequential Logic: Basic latch circuit, Debouncing of a switch, Flip-Flops: truth table and excitation table, conversion of Flip-flops, integrated circuit flip-flops. Race in sequential circuits,.	Chalk and Talk
5	9th & 10th week	Shift Registers, Counters - Synchronous, Asynchronous, Up-Down, Design of counters Analysis of clocked sequential circuits.	Chalk and Talk
6	11th & 12th week	Design with state equations, Moore and Mealy graphs, State reduction and assignment ,Sequence detection, Hazards.	Chalk and Talk
7	13th & 14th week	Programmable logic devices,Design using Programmable Logic Devices (ROM,PLA,PAL,FPGA). Digital Hardware: Logic levels, Digital integrated circuits, Logic delay times, Fan-Out and Fan-In,	Chalk and Talk
8	15th & 16th week	Logic families, TTL ECL. CMOS Electronics: CMOS electronics and Electronic logic gates, The CMOS inverter, Logic formation using MOSFETs, CMOS memories. Interfacing between different families.	Chalk and Talk

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage

1	Continuous Assessment1		12 weeks	20
2	Hands-on Test	6th week	1 Hour	20
3	Assessment 2	14th week	1 Hour	20
	Compensation Assessment	15th week	1 Hour	20
4	Final Assessment	18th week	3 Hours	40

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Written feedback from students
Students' performance in tests

COURSE POLICY (including compensation assessment to be specified)

COMPENSATION ASSESSMENT : Compensation assessment will be conducted for students who miss Assessment 2. Students should get permission from the faculty by giving valid reason in written form to write compensation assessment. No compensation Assessment for Hands on Test.

REASSESSMENT:

- Refer to B. Tech Regulations B.10.1 and B.12

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- At least 75% attendance in each course is mandatory.
- A maximum of 10% shall be allowed under On Duty (OD) category.
- Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

➢ The above policy against academic dishonesty shall be applicable for all the programmes.
ADDITIONAL INFORMATION, IF ANY
FOR APPROVAL
Course Faculty 8/8/23 **CC- Chairperson** _____ **HOD** _____

Guidelines

a) The number of assessments for any theory course shall range from 4 to 6.

b) Every theory course shall have a final assessment on the entire syllabus with at least 30% weightage.

c) One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered.

d) The passing minimum shall be as per the regulations.

B.Tech. Admitted in				P.G.
2018	2017	2016	2015	
35% or (Class average/2) whichever is greater.		(Peak/3) or (Class Average/2) whichever is lower		40%

e) Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.

f) Absolute grading policy shall be incorporated if the number of students per course is less than 10.

g) Necessary care shall be taken to ensure that the course plan is reasonable and is objective.