DEPARTMENT OF INSTRUMENTATION AND CONTROL ENGINEERING NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

	COURSE PLAN	I-PARTI	SALES ENTERED TO A
Name of the programme and specialization	B.Tech- Instrumentation and Control Engineering		
Course Title	Circuits and Digital Laboratory		
Course Code	ICLR11	No. of Credits	2
Course Code of Pre- requisite subject(s)	NIL	iv.	
Session	July 2023	Section	A
Name of Faculty	Dr. Shiraz Sohail	Department	ICE
Email	SSohail Onitteditelephone No.		- 9775550302
Name of Course Coordinator(s)	NA		(112330302
E-mail	NA	Telephone No.	NA
Course Type	Laboratory		

List of Experiments (approved in BoS)

- 1. Verification of Electrical Circuit laws and network theorems.
- 2. Time Response of RL, RC and RLC circuits.
- 3. Frequency Response of RL, RC and RLC circuits, resonance.
- 4. A.C. circuits and Network realization.
- 5. Design and verification of combinational logic circuits.
- 6. Design and verification of sequential logic circuits.

COURSE OBJECTIVES

- L_{ϵ} To introduce to the design of passive, bilateral electrical circuits,
- 2. To impart knowledge in network analysis and realization.
- 3. To impart knowledge in design and verification of combinational and sequential logic circuits.

COURSE OUTCOMES (CO)

On completion of this lab, the students will be able to,

- 1. Design and analyze electrical circuits based on circuit laws and network theorems.
- 2. Analyze the time domain response of RL, RC and RLC circuits.
- 3. Analyze the frequency domain response of RL, RC and RLC circuits.
- 4. Design and verify sequential and combinational logic circuits.

	Aligned Programme Outcomes (PO)	
 Design and analyze electrical circuits based on circuit laws and network theorems. 	1,2,3,5,7,12	
Analyze the time domain response of RL, RC and RLC circuits.	1,2,3,5,7,12	

- 1. Feedback from the students during the class committee meetings and at the mid of the semester
- 2. Feedback before end semester examination through a questionnaire

COURSE POLICY

MODE OF CORRESPONDENCE (email/phone etc) - Email

COMPENSATION ASSESSMENT POLICY

One Compensation Lab will be conducted on 11th week for students who miss lab session, provided they should get permission from the faculty by giving valid reason in written form

Grading Policy

- Relative grading will be used to decide the clusters (range) of the total marks scored. The passing minimum should be 35% or (Class average/2) whichever is greater.
- All the students are expected to finish all the 10 experiments. Students, who fail to complete at least 6 experiments, have to rejoin the course after a year along with next batch.

Reassessment Examination

- A student may be permitted to withdraw from appearing for the End Semester Examination for valid reasons on production of valid medical certificate and with the approval of Head of the Department. Withdrawal application shall be valid only if it is made before the commencement of the examination.
- For students who miss the final semester assessment, reassessment will be conducted for 30% mark and internal marks remain same.
- Those who failed in the laboratory course should register for reassesment examination which will be conducted for 100% mark (Absolute grading where passing minimum is 35).
- Grades for the students who have withdrawn from writing the end semester exam will be same as the regular assessment grades. For those who are failed or absent and appearing for reassessment, the maximum grade is restricted to 'E'.
- Reassessment exam will be conducted in the first week of the next semester or earlier during the vacation.
- Students who fail in reassesment exam have to register for formative assessment.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- At least 75% attendance in each course is mandatory.
- A maximum of 10% shall be allowed under On Duty (OD) category / valid reasons on production of valid medical certificate with the approval of Head of the Department.
- Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

3. Analyze the frequency domain response of RL, RC and RLC circuits.	1,2,3,5,7,12
4. Design and verify sequential and combinational logic circuits.	1,2,3,5,7,12

COURSE PLAN - PART II

COURSE OVERVIEW

This course provides experience in analysis of circuits. This laboratory course covers basic electrical circuit laws, network theorem, time and frequency response of RL, RC and RLC circuits, network analysis and sequential and combinational logic circuits.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
Ĭ.	1 st week	Instruction and introduction to lab experiments	Experiment
2	2 nd and 3 rd week	Basic Electrical Circuit laws	Experiment
3	4th week	Verification of network theorems	Experiment
4	5 th and 6 th week	RL, RC and RLC circuits – Time domain response.	Experiment
5	7th and 8th week	RC, RL and RLC circuits –Frequency domain response.	Experiment
6	9th week	Three phase circuits	Experiment
7	10 th week	Two port networks	Experiment
8	11th week	Logic gates and digital circuits	Experiment
()	12th week	Counters and shift registers	Experiment
10	13th week	Repeat class	Experiment
11	14 th week	Compensation class ★	Experiment

Final Assessment

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
L	Design calculation, simulation and result analysis	Every class	3 hours	50
СРА	Compensation Assessment*	3 rd week of November	3 hours	5
2	Viva / Quiz	4 th week of November	н;	20
3	Final Assessment	I st week of December	3 hours	30

COURSE EXIT SURVEY

ACADEMIC DISHONESTY & PLAGIARISM

- > Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- > Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- > The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the
- The above policy against academic dishonesty shall be applicable for all the

programmes.	against academic dishonesty shal	be applicable for all the
ADDITIONAL INFORMATIO	N, IF ANY	
Any suggestions, queries and	d feedback can be communicated thro	ough email (ssohail@nitt.edu)
FOR APPROVAL		- (see name (see an all each
Course Faculty	CC- Chairperson	HOD GOOD LAD
Dr. Shiraz Sohail	Dr. <u>Ramakalyan Ayyagari</u>	Dr. K Dhanalakshmi