DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE PLAN – PART I			
Name of the programme and specialization	**B.Tech- Electrical & Electronics Engineering**		
Course Title	**Digital System Design and HDLS**		
Course Code	**EEPE17**	**No. of Credits**	**3**
Course Code of Pre-requisite subject(s)	**EEPC14**		
Session	**July-2023**	**Section (if, applicable)**	**3rd year A & B**
Name of Faculty	**Ch. Chandra Sekhar Nidhi Chandrakar**	**Department**	**EEE**
Official Email	**407121004@nitt.edu 407121007@nitt.edu**	**Telephone No.**	**9494622603 9111349840**
Name of Course Coordinator(s) (if, applicable)			
Official E-mail		**Telephone No.**	
Course Type (please tick appropriately)	**Core course**	**Elective course** ✓	

Syllabus

Finite State machines - Mealy and Moore, state assignments, design and examples – Asynchronous finite state machines – design and examples – multi-input system controller design.

Programmable Devices: Simple and Complex Programmable logic devices (SPLD and CPLDs), Field Programmable Gate Arrays (FPGAs), Internal components of FPGA, Case study: A CPLD and a 10 million gates type of FPGA.

VHDL- Modeling styles – structural – Behavioral – Dataflow - Design of simple/ complex combinational and sequential circuits using VHDL – Data types – Test bench and simulation. Case study on system design.

Verilog HDL - Modeling styles – structural – Behavioral – Dataflow - Design of simple/ complex combinational and sequential circuits using Verilog – Test bench and simulation – case study on system design.

Fault classes and models – Stuck at faults, Bridging faults - Transition and Intermittent faults. Fault Diagnosis of combination circuits by conventional methods - Path sensitization technique - Boolean different method and Kohavi algorithm.

COURSE OBJECTIVES

To impart the concepts of Digital systems and hardware description languages.

MAPPING OF COs with Pos	
Course Outcomes	**Programme Outcomes (PO)**

1. Understand the insights of the finite state machines.
2. Appreciate and classify the programmable logic devices and FPGA.
3. Design the logic circuits using VHDL.
4. Develop the systems using Verilog HDL.
5. Test the circuits for different faults.

PO	CO_1	CO_2	CO_3	CO_4	CO_5
1	M	L	M	M	M
2	L	L	L	L	L
3	M	L	M	M	L
4	L	L	L	L	L
5	M	L	H	H	M
6	L	L	L	L	L
7	L	L	L	L	L
8	L	L	M	M	L
9	L	L	M	M	L
10	L	L	L	L	M
11	L	L	M	M	L
12	H	M	H	H	H

COURSE PLAN – PART II

COURSE OVERVIEW

8COURSE TEACHING AND LEARNING ACTIVITIES

S.No	Week/Contact Hours	Topic	Mode of Delivery
1.	Week 1 31st July -4th Aug 2023 (3 Contact hour)	Finite State machines - Mealy and Moore and Verilog HDL - Modeling styles	Chalk & Talk/PPT
2.	Week 2 7 Aug – 13 Aug 2023 (3 Contact hours)	Verilog HDL - Modeling styles and – structural – Behavioral – Dataflow	Chalk & Talk/PPT
3.	Week 3 14Aug- 20 Aug 2023 (3 Contact hours)	Asynchronous finite state machines – design and examples and Design of simple/ complex combinational and sequential circuits using Verilog	Chalk & Talk/PPT
4.	Week 4 21 Aug - 27 Aug 2023 (3 Contact hour)	Multi-input system controller design and Test bench and simulation. Case study on system design.	Chalk & Talk/PPT
5.	Week 5 28 Aug – 3 Sep 2023 (3 Contact hours)	Simple and Complex Programmable logic devices (SPLD and CPLDs) and VHDL- Modeling styles	Chalk & Talk/PPT
6.	Week 6 4 - 10 Sep 2023	First Assessment	

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7.	Week 7 11 – 17 Sep 2023 (3 Contact hours)	Field Programmable Gate Arrays (FPGAs) and – structural – Behavioral – Dataflow	Chalk & Talk/PPT
8.	Week 8 18 - 24 Sep 2023 (3 Contact hour)	Internal components of FPGA. Case study: A CPLD and a 10 million gates type of FPGA. And Design of simple/ complex combinational and sequential circuits using Verilog	Chalk & Talk/PPT
9.	Week 9 27 – 1 Oct	**Academic Break**	
10.	Week 10 2 - 8 Oct 2023 2023 (2 Contact hours)	Test bench and simulation case study on system design. **Second Assessment**	Chalk & Talk/PPT
11.	Week 11 9 - 15 Oct 2023 (3 Contact hours)	Fault classes and models	Chalk & Talk/PPT
12.	Week 12 16 - 22 Oct 2023 (3 Contact hours)	Stuck at faults, Bridging faults	Chalk & Talk/PPT
13.	Week 13 23 Oct - 29 Oct 2023 (2 Contact hours)	Transition and Intermittent faults	Chalk & Talk/PPT
14.	Week 14 30 Oct - 05 Nov 2023 (3 Contact hours)	Fault Diagnosis of combination circuits by conventional methods	Chalk & Talk/PPT
15.	Week 15 07 - 11 Nov 2023 (3 Contact hours)	***Compensation Assessment (CPA)*** Path sensitization technique Boolean different method	Chalk & Talk/PPT
16.	Week 16 14 - 18 Nov 2023 (3 Contact hours)	Kohavi algorithm	Chalk & Talk/PPT
17.	Week 18 27 Nov – 1 Dec 2023	Final Assessment.	

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week	Duration	% Weightage
1	I[st] Class Test	Week 6 4 – 10 Sep 2023	60 minutes	20
2	II[nd] Class Test	Week 10 2 - 8 Oct2023	60 minutes	20
3	Seminar/ Mini project	• Seminars: Presentation on topics related to Test the circuits for different faults. • Assignments		10+10=20
CPA	Compensation Assessment	Week 16 14Nov – 18 Nov2023	60 minutes	20
4	Final Assessment	Week 18 27 Dec – 1 Dec2023	180 minutes	40

ESSENTIAL READINGS: Textbooks, Refernce books, website address, journals,etc

Text Books:

1. William I. Fletcher, 'An Engineering Approach to Digital Design', Prentice Hall, 2009.
2. Donald D.Givone, 'Digital Principles and Design', Tata McGraw-Hill, 1st Edition, 2003.
3. Morris Mano, 'Digital Design', PHI, 3rd Edition, 2005.
4. J. Bhaskar, 'Verilog HDL Primer', BPB publications, 2000.

Reference Books:

1) Samuel C. Lee, 'Digital Circuits and Logic Design', PHI Learning, 1st Edition, 2008.

COURSE EXIT SURVEY

- Feedback from the students during class committee meetings
- Anonymous feedback through questionnaire (Mid of the semester & End of the semester)
- End semester feedback on course outcomes

COURSE POLICY (including compensation assessment to be specified)

1. Attending all the assessments mandatory for every student
2. One compensation assessment will be conducted for those students who are being physically absent for the assessment 1 and/or 2, only for the valid reason.
3. At any case CPA will not be considered as an improvement test.
4. Absolute/Relative grading will be adopted for the course.

ATTENDANCE POLICY(A uniform attendance policy as specified below shall be followed)

- At least 75% attendance in each course is mandatory.
- A maximum of 10% shall be allowed under On Duty (OD) category.

Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

The above policy against academic dishonesty shall be applicable for all the programs.

ADDITIONAL INFORMATION, IF ANY

FOR APPROVAL

Course Faculty

CC- Chairperson

HOD

11/08/23