DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	ELECTRICAL AND ELECTRONICS ENGINEERING		
Course Title	DIGITAL ELECTRONICS		
Course Code	EEPC14	**No. of Credits**	3
Course Code of Pre-requisite subject(s)	-		
Session	July 2023	**Section (if, applicable)**	A
Name of Faculty	Dr. S. Mageshwari	**Department**	EEE
Email	mageshwari@nitt.edu	**Telephone No.**	0431-2503260
Name of Course Coordinator(s) (if, applicable)	-		
Course Type	[√] Core course	[ ] Elective course	

Syllabus (approved in BoS)

Review of number systems, binary codes, error detection and correction codes. Digital Logic Families– Introduction to RTL, DTL, TTL, ECL and MOSL families – wired and operation, characteristics of digital logic family – comparison of different logic families.

Combinational logic representation of logic functions – SOP and POS forms, K-map representations –minimization using K-maps- simplification and implementation of combinational logic – multiplexers and demultiplexers – code converters, adders, subtractors.

Sequential logic- SR, JK, D and T flip-flops – level triggering and edge triggering – counters – Pulse forming circuits – asynchronous and synchronous type – Modulo counters – Shift registers – Ring counters.

Synchronous Sequential Logic circuits – state table and excitation tables – state diagrams – Moore and Mealy models – design of counters – analysis of synchronous sequential logic circuits – state reduction and state assignment.

Asynchronous sequential logic circuits-Transition table, flow table – race conditions – circuits with latches, analysis of asynchronous sequential logic circuits – introduction to design – implication table – hazards – programmable logic array and devices.

Text Books:

1. *Morris Mano.M, 'Digital Logic and Computer Design', Prentice Hall of India, 3rd Edition, 2005.*
2. *Donald D. Givone, 'Digital Principles and Design', Tata McGraw Hill, 1st Edition, 2003.*
3. *Thomas L Floyd, 'Digital fundamentals', Pearson Education Limited, 11th Edition, 2015.*

Reference Books:

1. *Tocci R.J., Neal S. Widmer, 'Digital Systems: Principles and Applications', Pearson Education Asia, 2014.*
2. *Donald P Leach, Albert Paul Malvino, Goutam Sha, 'Digital Principles and Applications', Tata McGraw Hill, 7th Edition, 2010.*

COURSE OBJECTIVES
This subject exposes the students to digital fundamentals
COURSE OUTCOMES (CO)
Course Outcomes
1.Interpret, convert and represent different number systems
2.Manipulate and examine Boolean algebra, logic operations, Boolean functions and their simplification.
3.Design and analyze combinational and sequential logic circuits

Mapping of Programme outcomes with Course outcomes:

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	1	1	1	1	1	3	3	3	1	3
CO2	2	2	1	1	1	1	1	3	3	3	1	3
CO3	3	2	3	1	2	1	3	3	3	3	3	3

COURSE PLAN – PART II

COURSE OVERVIEW

This is a basic course to teach Digital fundamentals which starts with number systems and move further into the different logic circuits like combinational and sequential in detail.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1	1(two hours)	Review of number systems	C&T,PPT
2	1(one hour), 2 (one hour)	Binary codes – BCD and computations	C&T,PPT
3.	2 (two hours), 3(two hours)	Error detection and correction codes.	C&T,PPT
4.	3(one hour)	*Objective Test*	
5.	4 (three hours)	Combinational logic – representation of logic functions – SOP and POS forms K-map representations – minimization using K maps	C&T,PPT
6.	5(two hours)	simplification and implementation of combinational logic – multiplexers and demultiplexers	C&T,PPT
7.	5(one hour) 6(two hours)	code converters,	C&T,PPT
8.			
9.	6(one hour)	adders, subtractors	C&T,PPT
10.	7(two hours)	Digital Logic Families: TTL and MOSL	C&T,PPT
11	7(one hour), 8 (three hours), 9 (three hours)	Sequential Logic – SR,JK,D and T flip flops-level triggering and edge triggering counters – asynchronous and synchronous type – Modulo counters	(Flip-class), PPT
		Objective cum Design Test 1	
12.	10 (two hours)	Shift registers – Ring counters.	
13.	10 (one hour), 11(one hour)	Synchronous Sequential Logic circuits-state table and excitation tables-state diagrams *Objective cum Design Test 2*	(Flip-class),PPT

14.	11(Two hour)	**Moore and Mealy models**	
15.	12 (Two Hours)	*Analogy Model Evaluation*	
16.	12 (one hour)	**Design of counters-analysis of synchronous sequential logic circuits-state reduction and state assignment.**	(Partly Flip-class)
17.	13 (three hours)	**Asynchronous sequential logic circuits-Transition table, flow table – race conditions – circuits with latches, analysis of asynchronous sequential logic circuits.**	(Partly Flip-class), PPT
18.	14 (two hours)	**Introduction to design – implication table – hazards.**	
19.	14(one hour), 15 (three hours)	*Real time working model Evaluation* **Programmable logic array and devices.**	
20.	16(one hour)	*Compensation Assessment (CPA)*	

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Objective Test	3	One hour	10
2	Objective Cum Design Test1	6	One hour	15
3	Objective Cum Design Test2	9	One hour	15
4	Analogy Model Evaluation	11	One hour	10
5	Real time working model Evaluation	14	One hour	10
CPA	*Compensation Assessment**	*16*	*One hour*	*15*
6	Final Assessment	End of semester	Three hours	40

*** If any student is not able to attend any of the continuous assessments CAs: 1 ,2 and 3(refer Sl. Nos. in course assessment methods) due to genuine reason.**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings
Anonymous feedback through questionnaire
End semester feedback on Course Outcomes

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

MODE OF CORRESPONDENCE (email/ phone etc)

1. **All the students are advised to check their WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through their webmail only.**
2. **Queries (if required) to the course teacher shall only be emailed to digital.eee.nitt@gmail.com**

COMPENSATION ASSESSMENT POLICY

1. **Attending all the assessments are MANDATORY for every student.**
2. **If any student is not able to attend any of the continuous assessments CAs: 1,2 and 3 (refer Sl. Nos. in course assessment methods) due to genuine reason, student is permitted to attend the compensation assessment (CPA) with % weightage equal to maximum of the CAs. However, maximum of the % weightage among the assessments for which the student was absent will be considered for computing marks for CA.**
3. **At any case, CPA will not be considered as an improvement test.**
4. **The minimum marks for passing this course and grading pattern will adhere to the regulations of the Institute.**

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- **Attending all the classes for this course is mandatory.**
- **Attendance policy will be as per the Institute's regulation.**

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

The Course Coordinator is available for consultation at times that is displayed on the coordinator's office notice board.

Queries may also be emailed to the Course Coordinator directly at digital.eee.nitt@gmail.com

FOR APPROVAL

Course Faculty S. Magesh **CC-Chairperson** C Nagamani 3/8/'23 **HOD** 03/08/23