DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Course Title	Design of Embedded Controllers for Smart Micro-grid		
Course Code	EE704	No. of Credits	03
Course Code of Pre-requisite subject(s)	-	M.Tech Power Electronics	
Session	~~July~~/ Jan. 2023	Section	~~A / B~~
Name of Faculty	Dr. S. Moorthi	Department	EEE
Email	moorthi.embeddedsystems@gmail.com	Telephone No.	0431-2503267
Name of Course Coordinator(s)	--		
Course Type	☐ Core course	☑ Elective course	

Syllabus (approved in BoS)

Embedded System Architectures–ARM processor and SHARC processor-architectural designmemory organization- data operation –bus configurations. System on-chip, scalable bus architectures, Design example: Alarm clock, hybrid architectures.

Sensors and Special ICs – Voltage Sensor, Current Sensor, Speed Sensor, RMS calculation IC, Battery Management IC, Opto-couplers and Current amplification transistors.

Real time operating systems(RTOS)–real time kernel– OS tasks–task states– task scheduling–interrupt processing – Embedded Networks –Distributed Embedded Architecture– Hardware and Software Architectures, Networks for embedded systems– I2C, CANBus, Ethernet, Internet, Network– Based design– Design Example: Elevator Controller.

Typical FPGA board qualitative analysis: FPGA IC interfacing with peripherals: ADC, DAC, display (LED, LCD), Communication networks like Ethernet.

Study of a Smart Micro-grid model – Sensors interfacing with FPGA board – Design of Source and Load Controllers – Communication between the controllers – Concepts of Source and Load management.

Reference Books:

1. Wayne Wolf, 'Computers as Components: Principles of Embedded Computing System Design', Morgan Kaufman Publishers,3rd Edition, 2012.
2. C.M.Krishna, Kang G. Shin ,'Real time systems', McGrawHill,2010.
3. Herma K., Real Time Systems: Design for Distributed Embedded Applications, Kluwer Academic, 2ndEdition, 2011.
4. WilliamHohl, 'ARM Assembly Language, Fundamentals and Techniques', CRC Press, 2009
5. Nazzareno Rossetti, "Managing Power Electronics: VLSI and DSP-driven Computing systems:, Wiley-Interscience Publications, 2006.
6. Krzysztof Iniewski, "Smart Grid Infrastructure & Networking", Mc-Graw Hill Education (India) Limited, 2012.

COURSE OBJECTIVES

To enable the learner to understand the concepts of embedded controllers with its Application to smart grids.

COURSE OUTCOMES (CO)

Upon completion of the course, the students will be able to	Aligned Programme Outcomes (PO)
1. Understand the architecture of Embedded systems	PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PO12, PO13, PO14.
2. Explore the possible peripherals with the processor	
3. Acquire the knowledge of requirements of the real time OS and embedded networks.	
4. Appraise the typical use of FPGA as embedded controller	
5. Apply the concepts of embedded controllers for smart grid	

COURSE PLAN – PART II

COURSE OVERVIEW

This is a course to teach the design of embedded controllers which are mainly required for the development of Digital Controllers for Power Electronic applications.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1.	1 (two contact hours)	Embedded System Architectures	C&T
2.	1 (one contact hour), 2	ARM processor and SHARC processor	C&T
3.	3 (two hours)	Architectural design, memory organization- data operation, bus configurations	(Flip-class)
4.	3 (one hour), 4 (one contact hours)	System on-chip, scalable bus architectures, Design example: Alarm clock, hybrid architectures.	C&T
5.	4 (one contact hour)	*Objective test*	-
6.	4 (one contact hour)	Sensors and Special ICs	PPT
7.	5 (two contact hours)	Voltage Sensor, Current Sensor, Speed Sensor	PPT
8.	6 (one contact hour)	RMS calculation IC, Battery Management IC	PPT
9.	6 (two hours)	Opto-couplers and Current amplification transistors.	PPT, C&T
10.	8 (two hours)	Real time operating systems(RTOS), Real time kernel, OS tasks, task states, task scheduling, interrupt processing *Written Test*	C&T, PPT
12.	8 (one hour), 9	Embedded Networks, Distributed Embedded Architecture, Hardware and Software Architectures	C&T, PPT
13.	10(two hours)	Networks for embedded systems, I2C, CAN Bus, Ethernet, Internet, Network Based design, Design Example: Elevator Controller	C&T,PPT (Flip-class)
14.	10 (one hour)	*Group task evaluation*	
15.	11, 12 (two hours)	Typical FPGA board qualitative analysis: FPGA IC interfacing with peripherals: ADC, DAC, display (LED, LCD), Communication networks like Ethernet.	C&T, PPT (partly Flip-class)
16.	12 (one hour)	*Real time systems – seminar presentation*	
17.	13, 14 (two hours)	Study of a Smart Micro-grid model, Sensors interfacing with FPGA board, Design of Source and Load Controllers	C&T, PPT
18.	14 (one hour), 15	Concepts of Source and Load management.	C&T, PPT
19.	16 (one hour)	*Compensation Assessment (CPA)*	
		Final Written Exam	

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Objective test	02	One hour	10
2.	Written test	08	One hour	15
3.	Group task	10	One hour	20
4.	Real time systems - seminar presentation	12	One hour	15
	Compensation Assessment (CPA)	16	One hour	15*
5.	Final Written Exam	End of semester	Two hours	40

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings

Anonymous feedback through questionnaire (Mid of the semester & End of the semester)

End semester feedback on Course Outcomes

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, , academic honesty and plagiarism etc.)

MODE OF CORRESPONDENCE (email/ phone etc)

1. **All the students are advised to check their NITT WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through their webmail only.**
2. **Queries (if required) to the course teacher shall only be emailed to drmoorthi.vlsi@gmail.com**

ATTENDANCE

Attendance will be taken by the faculty in all the contact hours.

- **At least 75% attendance in each course is mandatory.**
- As per institute norms.

COMPENSATION ASSESSMENT

1. **Attending all the assessments are MANDATORY for every student.**
2. **If any student is not able to attend any of the continuous assessments (CAs : 1, 2 only) due to genuine reason, student is permitted to attend the compensation assessment (CPA) with % weightage equal to maximum of the CAs. However, maximum of the % weightage among the assessments for which the student was absent will be considered for computing marks for CA.**
3. **At any case, CPA will not be considered as an improvement test.**
4. **The minimum marks for passing this course and grading pattern will adhere to the regulations of the Institute.**

ACADEMIC HONESTY & PLAGIARISM

1. **Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.**
2. **Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.**
3. **The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.**
4. **The above policy against academic dishonesty shall be applicable for all the programmes.**
5. **Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.**

ADDITIONAL INFORMATION

The faculty is available for consultation at times as per the intimation given by the faculty.

Queries may also be emailed to the Course Coordinator directly at moorthi.embeddedsystems@gmail.com

FOR APPROVAL

Course Faculty 18/1/2023 **CC-Chairperson** **HOD** 02/02/23