DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I

Name of the programme	B.Tech. ELECTRICAL AND ELECTRONICS ENGINEERING		
Course Title	EMBEDDED SYSTEM DESIGN		
Course Code	EEPE28	No. of Credits	3
Course Code of Pre-requisite subject(s)	EEPC22	B.E/B.Tech (VIII Semester)	
Session	January 2023	Section	A&B
Name of Faculty	Dr. S. Moorthi	Department	EEE
Email	moorthi.embeddedsystems@gmail.com	Telephone No.	0431-2503267
Name of Course Coordinator(s)	-		
Course Type	☐ Core course	☑ Elective course	

Syllabus (approved in BoS)

Embedded System Architectures – ARM processor and SHARC processor - architectural design – memory organization -data operation-bus configurations. System on-chip, scalable bus architectures, Design example: Alarm clock, hybrid architectures.

Sensor and Actuator I/O – ADC, DAC, timers, Servos, Relays, stepper motors, H-Bridge, CODECs, FPGA, ASIC, diagnostic port.

Real time operating systems (RTOS) – real time kernel – OS tasks – task states – task scheduling – interrupt processing – clocking communication and synchronization – control blocks – memory requirements and control – kernel services.

Embedded Networks – Distributed Embedded Architecture – Hardware and Software Architectures, Networks for embedded systems– I2C, CAN Bus, Ethernet, Internet, Network-based design– Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

System Design – Specification, Requirements and Architectural design of PBX systems, Set-top box, Ink-jet printer, Laser printer, Personal digital Assistants.

Text Books:

1. Wayne Wolf, 'Computers as Components: Principles of Embedded Computing System Design', Morgan Kaufman Publishers, 2nd Edition, 2010.
2. C.M Krishna, Kang G. Shin, 'Real time systems', Mc-Graw Hill, 1st Edition, 2010.
3. Galski D. Vahid F., Narayan S., 'Specification and Design of Embedded Systems', Prentice Hall, 1st Impression, 2007.

Reference Books:

1. Herma K., 'Real Time Systems: Design for Distributed Embedded Applications', Springer, 2nd Edition, 2011.
2. William Hohl, 'ARM Assembly Language, Fundamentals and Techniques', CRC Press, 2009.

COURSE OBJECTIVES

To enable the learner to design a system with combination of hardware and software for a specific application.

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)
1. Remember the concepts of process and controllers.	PO1, PO2, PO3, PO6, PO8, PO9, PO10, PO13.
2. Apply the concepts for real-time applications	
3. Create a real-time system for particular applications.	

COURSE PLAN – PART II

COURSE OVERVIEW

This is an advanced course which teaches both hardware and software required for the design of an embedded system with real time applications.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1	1(two hours)	Embedded System Architectures	C&T
2	1(one hour), 2 (one hour)	Architectural design, memory organization	C&T
3.	2 (two hours), 3(two hours)	System on-chip, scalable bus architectures Design example: Alarm clock, hybrid architectures.	C&T
4.	3(one hour)	*Objective Test*	C&T
5.	4 (three hours)	Sensor and Actuator I/O, ADC, DAC,	C&T
6.	5(two hours)	Timers, Servos, Relays,	C&T
7.	5(one hour)	Stepper motors, H-Bridge, CODECs,	C&T
8.	6(two hours)		
9.	6(one hour)	FPGA	C&T
10.	7(two hours)	ASIC, diagnostic port *Written Test*	C&T
11	7(one hour), 8 (three hours), 9 (three hours)	Real time operating systems (RTOS), Real time kernel, OS tasks, task states, task scheduling, interrupt processing, clocking communication and synchronization	(Flip-class), PPT
12.	10 (two hours)	control blocks, Memory requirements and control, Kernel services.	C&T
13.	10 (one hour), 11(one hour)	Embedded Networks. Distributed Embedded Architecture, Hardware and Software Architectures, Networks for embedded systems,	(Flip-class),PPT
14.	11(one hour)	I2C, CAN Bus	C&T
15.	11(one hour)	*Group Task Evaluation*	
16.	12(three hours)	Ethernet, Internet, Network-based design, Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.	PPT (Partly Flip-class)
17.	13 (three hours)	System Design – Specification, Requirements and Architectural design of PBX systems,	PPT
18.	14(two hours)	Set-top box, Ink-jet printer	C&T
19.	14(one hour), 15 (three hours)	*Presentation on real time systems* Laser printer, Personal digital Assistants	C&T
20.	16(one hour)	*Compensation Assessment (CPA)*	

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Objective Test*	3	One hour	10
2	Written Test*	6	One hour	15
3	Group task (2 members)	9	Two Hours	20
4	Presentation on real time systems	11	One hour	15
CPA	*Compensation Assessment**	*16*	*One hour*	*20*
5	Final Assessment	End of semester	Three hours	40

* If any student is not able to attend any of the continuous assessments CAs: 1 and 2 (refer Sl. Nos. in course assessment methods) due to genuine reason.

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings
Anonymous feedback through questionnaire
End semester feedback on Course Outcomes

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

MODE OF CORRESPONDENCE (email/ phone etc)

1. All the students are advised to check their WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through their webmail only.
2. Queries (if required) to the course teacher shall only be emailed to digital.eee.nitt@gmail.com

COMPENSATION ASSESSMENT POLICY

1. Attending all the assessments are MANDATORY for every student.
2. If any student is not able to attend any of the continuous assessments CAs: 1 and 2 (refer Sl. Nos. in course assessment methods) due to genuine reason, student is permitted to attend the compensation assessment (CPA) with % weightage equal to maximum of the CAs. However, maximum of the % weightage among the assessments for which the student was absent will be considered for computing marks for CA.
3. At any case, CPA will not be considered as an improvement test.
4. The minimum marks for passing this course and grading pattern will adhere to the regulations of the Institute.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- **Attending all the classes for this course is mandatory.**
- **Attendance policy will be as per the Institute's regulation for offline classes.**

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

The Course Coordinator is available for consultation at times that is displayed on the coordinator's office notice board.

Queries may also be emailed to the Course Coordinator directly at moorthi.embeddedsystems@gmail.com

FOR APPROVAL

Course Faculty 18/2/2023 **CC-Chairperson** **HOD** 06/02/23