NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE PLAN – PART I			
Name of the programme and specialization	III Year B.Tech, EEE		
Course Title	POWER ELECTRONICS		
Course Code	EEPC 19	No. of Credits	04
Course Code of Pre-requisite subject(s)	MAIR32, EEPC10 & EEPC13		
Session	July 2022	Section (if, applicable)	B
Name of Faculty	Dr. P. Srinivasa Rao Nayak	Department	EEE
Email	psnayak@nitt.edu	Telephone No.	7708243070
Name of Course Coordinator(s) (if, applicable)	Dr Manoranjan Sahoo		
Course Type (please tick appropriately)	☐ General Institute Requirement (GIR) ☑ Branch Specific Course		

Syllabus (approved in BoS)

Power Semiconductor Devices –power diodes, power transistors, SCRs, TRIAC, GTO, power MOSFETs, IGBTs-Principles of operation, characteristics, ratings, protection and gate drive circuits.

Controlled rectifiers- single- phase and three-phase- power factor improvement - dual converters.

DC-DC converters- Buck, Boost, Buck-Boost- with circuit configuration and analysis.

DC-AC converters- single-phase/three-phase, VSI, CSI, frequency and voltage control.

AC-AC converters- single/three-phase controllers, phase control, PWM AC voltage controller, Principle o f ON-OFF control and cyclo-converters.

COURSE OBJECTIVES

This course aims to equip the students with a basic understanding of modern power semiconductor devices, various important topologies of power converter circuits for specific types of applications. The course also equips students with an ability to understand and analyze non-linear circuits involving power electronic converters.

MAPPING OF COs with PO's	
Course Outcomes	**Programme Outcomes (PO)** (Enter Numbers only)
Upon completion of the course, the student will be able to 1. Understand the principle of operation of commonly employed power electronic converters. 2. Analyze non-linear circuits with several power electronic switches. 3. Equipped to take up advanced courses in Power Electronics and its application areas.	**1, 2, 3, 4,7,8, 9, 12,14**

COURSE PLAN – PART II

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1	Week 1 (Lectures) 10-12 August	Introduction	**Chalk & Board, PPT**
2	Week 2 (Lectures) 15-19 August	Introduction to Power Semiconductor Devices –power diodes, power transistors	**Chalk & Board, PPT**
3	Week 3 (4 Lectures) 22-26 April	TRIAC, GTO, power MOSFETs, IGBTs-Principles of operation, characteristics, ratings.	**Chalk & Board, PPT**
4	Week 4 (4 Lectures) 29 August-02 September	SCRs,Principles of operation, characteristics, ratings,protection and gate drive circuits.	**Chalk & Board, PPT**
5	Week 5 (4 Lectures) 05-09 September	Controlled rectifiers- single- phase	**Chalk & Board, PPT**
6	Week 6 (4 Lectures) 12-16 September	Controlled rectifiers-three-phase- power factor improvement	**Chalk & Board, PPT**
7	Week 7 (4 Lectures) 19–23 September	Dual converters & **First Assessment**	**Chalk & Board, PPT**
8	Week 8 (4 Lectures) 26-30 September	Introduction to DC-DC converters & Buck Operation	**Chalk & Board, PPT**

9	Week 9 (4 Lectures) 03-07 October	Boost, Buck-Boost- with circuit configuration and analysis.	**Chalk & Board, PPT**
10	Week 10 (4 Lectures) 10-14 October	DC-AC converters- single-phase/three-phase	**Chalk & Board, PPT**
11	Week 11 (4 Lectures) 17-21 October	VSI, CSI & **Second Assessment**	**Chalk & Board, PPT**
12	Week 12 (4 Lectures) 24-28 October	frequency and voltage control.	**Chalk & Board, PPT**
13	Week 13 (4 Lectures) 31October-04 November	AC-AC converters- single/three-phase controllers,	**Chalk & Board, PPT**
14	Week 14 (4 Lectures) 07-11 November	phase control of AC-AC converters	**Chalk & Board, PPT**
15	Week 15 (4 Lectures) 14-18 November	PWM AC voltage controller, Principle of ON-OFF control	**Chalk & Board, PPT**
16	Week 16 (4 Lectures) 21-25 November	cyclo-converters & **Third Assessment**	**Chalk & Board, PPT**
17	Week 17 (4 Lectures) 28-30 November	Numereical Problems & **Compensation Assessment**	**Chalk & Board, PPT**

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	**Assessment I (CT1)**	Week 8 26-30 September	1hr.15min	**25%**
2.	**Assessment II (CT2)**	Week 11 17-21 October	1hr.15min	**25%**
3.	**Surprise test / report / viva/Assignment**	Week 16 21-25 November	-	**10%**
	Compensation Assessment (Written test)	Week 17 28-30 November	1hr.15min	**80% of CT1/CT2**
4	**Final Assessment**	Week 17 28-30 November	3 hours	**40%**

ESSENTIAL READINGS : Textbooks, reference books Website addresses, Journals, etc

Text Books:

1.Rashid, M.H, 'Power Electronics - Circuits, Devices and Applications', Prentice Hall Publications, 3rd Edition, 2003.

2. M.D.Singh and K.B.Khanchandani, 'Power Electronics', Tata McGraw-Hill Publishing Company Limited, 2nd Edition, 2006.

3. Ned Mohan, Tore M. Undeland, William P. Robbins, 'Power Electronics', John Wiley & Sons Publications, 3rd Edition, 2006.

Reference Books:

1. Vedam Subramaniam, 'Power Electronics', New Age International (P) Ltd Publishers, 2001.

2. Philip T. Krein, 'Elements of Power Electronics', Oxford University Press, 1st Edition, 2012.

3. V.R.Moorthi, 'Power Electronics- Devices, Circuits and Industrial Applications', Oxford University Press, 1st Edition, 2005.

4. P.S. Bimbhra, 'Power Electronics', Khanna Publishers, 3rd Edition, 13th Reprint, 2004.

COURSE EXIT SURVEY

- Feedback from the students during class committee meetings
- Anonymous feedback through questionnaire

COURSE POLICY

- All students are expected to attend all the classes & laboratory sessions, Compensation Examination shall have 80% weightage.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- At least 75% attendance in each course is mandatory.
- A maximum of 10% shall be allowed under On Duty (OD) category.
- Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.

- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.
- The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION, IF ANY

FOR APPROVAL

Course Faculty _____ 22/11/2022 **CC- Chairperson** _____ **HOD** _____ 23/11/22

Guidelines

a) The number of assessments for any theory course shall range from 4 to 6.

b) Every theory course shall have a final assessment on the entire syllabus with at least 30% weightage.

c) One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered.

d) A student must score a minimum of 20% in the final assessment (for all courses) to complete the course.

e) The passing minimum shall be as per the regulations.

B.Tech. Admitted in				P.G.
2019	2018	2017	2016	
35% or (Class average/2) whichever is greater.			(Peak/3) or (Class Average/2) whichever is lower	35% or (Class average/2) whichever is greater.

f) Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.

g) Absolute grading policy shall be incorporated if the number of students per course is less than 10.

h) Necessary care shall be taken to ensure that the course plan is reasonable and is objective.