NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE PLAN – PART I			
Name of the programme and specialization	**III Year B.Tech, EEE**		
Course Title	**INTEGRATED CIRCUITS LABORATORY**		
Course Code	**EELR14**	**No. of Credits**	**02**
Course Code of Pre-requisite subject(s)	**EEPC21**		
Session	**July 2022**	**Section (if, applicable)**	**B**
Name of Faculty	**Dr. Aneesa Farhan M A**	**Department**	**EEE**
Email	aneesa@nitt.edu **aneesafma@gmail.com**	**Telephone No.**	**7598164452** **8015877137**
Name of Course Coordinator(s) (if, applicable)	**N A**		
Course Type (please tick appropriately)	☑ **Essential Laboratory Requirement (ELR)**		

Syllabus (approved in BoS)

- Understanding of Op-Amp Imperfections
- Linear Applications of Op-Amp
- Non-Linear Applications of Op-Amp
- Design of Active filters using Op-Amp
- Analog-to-Digital Conversion
- Digital-to-Analog conversion
- Timing circuits using 555 Timer
- Combinational and Sequential logic circuits
- Design of Code converter with seven-segment display
- Mini-Project

COURSE OBJECTIVES

The main objective of the course is to enable the students to gain an insight into the operation of basic integrated circuits. The course also equips the students to test and evaluate the effect of design parameters on the performance of the circuits such as operational amplifier-based Waveform generators, Timers, Filter circuits, ADC, DAC etc.

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Course Outcomes

Upon completion of the course, the students will be able to

1. Understand the non-ideal behavior of Op-amp.
2. Analyze and prepare the technical report on the experiments carried out.
3. Design application-oriented circuits using Op-amp and 555 timer ICs.
4. Create and demonstrate live project using ICs.

Programme Outcomes (PO) (Enter Numbers only)

COs / POs		Course outcomes (COs)			
		1	2	3	4
Programme Outcomes (POs)	1	M	H	H	M
	2	M	H	H	H
	3	H	L	H	H
	4	M	M	M	L
	5	NA	NA	NA	NA
	6	NA	NA	NA	M
	7	M	M	H	H
	8	M	M	M	M
	9	M	L	L	L
	10	M	L	L	M
	11	NA	NA	NA	NA
	12	H	H	H	H
	13	M	H	H	H
	14	M	L	H	M

COURSE PLAN – PART II

COURSE OVERVIEW

Integrated circuits gained a tremendous growth in most of the application because of the significant advantages like low power consumption, possibility for high speed communication, flexibility, low cost, miniaturization of hardware has led to greater processing standards & higher memory capacities with lesser area & more access speed.

The course is designed such that the initial experiments are to understand the basic operation and imperfections in op-amp ICs. The subsequent experiments are to design and implement various applications of op-amp. Thus, on the completion of the course, the students will be able to design and implement several real time applications using op-amp. This course also aims to apply the mathematical skills to a number of practical applications.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1	Week 1 10 August-12 August	Introduction to Linear Integrated Circuits and the laboratory course plan, methodology and evaluation	**Lecture**
2	Week 2 15 August – 19 August	Basic operation of op-amp: Inverting Amplifier :Gain {Ac and AC/DC) Linearity Frequency Response	Experimentation
3	Week 3 22 August -26 August	Basic operation of op-amp: Non-Inverting Amplifier And Opamp Imperfections	Experimentation
4	Week 4 29 Aug –2 september	Linear operations of op-amp Summing Amplifier Differential Amplifier	Experimentation
5	Week 5 5th -9th September	Linear operations of op-amp Integrator Differentiator	Experimentation
6	Week 6 12th -16th September	Precision Rectifiers	Experimentation
7	Week 7 19th -23th September	**Assessment II**	**Viva**
8	Week 8 26th -30th September	Design of high pass filter	Experimentation
9	Week 9 3th -7th October	Design of Low pass filter	Experimentation
10	Week 10 10 th -14 th October	Waveform Generators Triangular wave generator using 741	Experimentation
11	Week 11 17 th to 21 October	Analog to Digital Conversion	Experimentation

13	Week 12 24 th to 28 October	Digital to Analog Conversion	Experimentation
14	Week 13 01 th to 04 November	Timing Circuits using Timing IC 555	Experimentation
15	Week 13 07 th to 11 November	**Assessment II**	**Viva/Simulation**
16	Week 14 14 th -18 th November	**Assessment II contd.**	**. Viva/Simulation**
17	Week 15 21-25 November	**Compensation**	Experimentation
	Week 16. 28 to 30 November	**Assessment III**	**Lab Examination**

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Type of assessment	Duration	% Weightage
1.	**Assessment I**	Evaluation of Experimentation on every lab session	8 sessions	**50%**
2.	**Assessment II**	Oral viva	Two sessions	**20%**
3.	**Assessment III**	Lab Examination	1-2 hours	**30%**

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

1. Gayakwad R.A., 'Op-amps & Linear Integrated Circuits', Prentice Hall of India, New Delhi, 4th Edition, 2009.
2. Roy Choudhury and Shail Jain, 'Linear Integrated Circuits', 4th Edition, New Age International Publishers, 2010.
3. Sergio Franco,' Design with Operational Amplifiers and Analog Integrated Circuits', Tata McGraw Hill, 3rd Edition, 2002.
4. Sedra Smith, 'Microelectronic Circuits', Oxford University Press, 6th Edition, 2009.
5. R P Jain, 'Modern Digital Electronics', Tata McGraw-Hill Education, 3rd Edition, 2003

COURSE EXIT SURVEY

- Feedback from the students during class committee meetings
- Anonymous feedback through questionnaire

COURSE POLICY

- All students are expected to attend all the laboratory sessions
- Students who are absent during regular laboratory sessions have to redo the experiments by their own efforts.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- At least 75% attendance in each course is mandatory.
- A maximum of 10% shall be allowed under On Duty (OD) category.
- Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.
- The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION, IF ANY

FOR APPROVAL

Course Faculty _____ **CC- Chairperson** _____ 24/08/22 **HOD** _____