DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Course Title	**Principles of VLSI Design**		
Course Code	**EE 688**	**No. of Credits**	**03**
Course Code of Pre-requisite subject(s)	**-**	**Common for M.Tech. Power Electronics and Power Systems.**	
Session	**January 2022**	**Section**	**~~A / B~~**
Name of Faculty	**Dr. S. Moorthi**	**Department**	**EEE**
Email	**srimoorthi@nitt.edu**	**Telephone No.**	**0431-2503267**
Name of Course Coordinator(s) (if, applicable)	**--**		
Course Type	**Core course**	**√**	**Elective course**

Syllabus (approved in BoS)

MOS and Fabrication: VLSI technology- NMOS, CMOS and BICMOS circuit fabrication - Comparison of IC technologies - Operation characteristics, design equations, models and second order effects of MOS transistors - Fabrication of resistors and capacitors - Latch up, driver circuits.

Hardware Description languages: VHDL- Modeling styles – Design of simple / complex circuits using VHDL - Overview of Verilog HDL - Design of simple circuits using Verilog HDL.

CMOS Logic Circuits: Implementation of logic circuits using MOS and CMOS, Pass transistor and transmission gates, design of combinational and sequential circuits – Memory design.

Programmable Devices: Simple and Complex Programmable logic devices (SPLD and CPLDs) - Field Programmable Gate Arrays (FPGAs) - Internal components of FPGA - Case study: A CPLD and a 10 million gates type of FPGA.

ASIC: Types of ASICs - Design flow - Programmable ASICs - Programmable ASIC logic cells and interconnect for Xilinx and Altera families.

Reference Books:

1. Neil Weste, David Harris, 'CMOS VLSI Design: A Circuits and Systems Perspective', Addison-Wesley, 4th Edition, 2010.
2. M. J. Smith, 'Application Specific Integrated Circuits', Addison Wesley, 1997.
3. Uyemura, 'Introduction to VLSI Circuits and Systems', Wiley, 2002.
4. J. Bhaskar, 'A Verilog HDL Primer', Star Galaxy, 2nd Edition, 2000.

COURSE OBJECTIVES

Enables the student to get exposure on low power electronic system design and its application.

COURSE OUTCOMES (CO)

Upon completion of the course, the students will be able to	**Aligned Programme Outcomes (PO)**
1. Understand the concepts and characteristics of MOS devices.	**PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PO12, PO13, PO14.**
2. Model the system using Hardware Description languages.	
3. Design the CMOS logic circuits and memory units.	
4. Acquire knowledge on PLDs.	
5. Appraise the possibilities of ASIC design.	

COURSE PLAN – PART II			
COURSE OVERVIEW			
This is a course to teach the design of low power electronic circuits which are mainly required for the development of Digital Controllers for Power Electronic applications.			
COURSE TEACHING AND LEARNING ACTIVITIES			
S.No.	**Week/Contact Hours**	**Topic**	**Mode of Delivery**
1.	**1 (two contact hours)**	**Review of Electronics fundamentals**	**C&T**
2.	**1 (one contact hour), 2**	**Implementation of logic circuits using nMOS and CMOS devices**	**C&T**
3.	**3 (two hours)**	**Pass transistor and transmission gates**	**PPT**
4.	**3 (one hour), 4 (one contact hour)**	**memory design**	**C&T**
5.	**4 (one contact hour)**	*Objective test*	**-**
6.	**4 (one contact hour)**	**Simple and Complex Programmable logic devices (SPLD and CPLDs)**	**PPT**
7.	**5 (two contact hours)**	**Design problems in PLDs**	**PPT**
8.	**6 (one contact hour)**	**Field Programmable Gate Arrays (FPGAs), Internal components of FPGA.**	**PPT**
9.	**6 (two hours)**	**Guest Lecture about recent FPGAs from company.**	**PPT, C&T**
10.	**8 (two hours)**	**VHDL- Modeling styles – structural – Behavioral – Dataflow.** *Circuit Design Test*	**C&T, PPT**
12.	**8 (one hour), 9**	**Design of simple/ complex combinational and sequential circuits using VHDL.**	**C&T, PPT**
13.	**10(two hours)**	**Data types – Test bench and simulation.**	**C&T,PPT**
14.	**10 (one hour)**	*Group Assignment*	
15.	**11, 12 (two hours)**	**Verilog HDL - Modeling styles – structural – Behavioral – Dataflow - Design of simple/ complex combinational and sequential circuits using Verilog, Testbench and Simulation.**	**C&T, PPT (partly Flip-class)**
16.	**12 (one hour)**	*Simulation Test*	
17.	**13, 14 (two hours)**	**Operation characteristics, design equations, models and second order effects of MOS transistors, Fabrication of resistors and capacitors. Latch up, Driver circuits.**	**C&T, PPT**
18.	**14 (one hour), 15**	***ASIC:*** **Types of ASICs-Design flow-Programmable ASICs-Programmable ASIC logic cells and interconnect for Xilinx and Altera families.**	**Flip-class and VC**
19.	**16 (one hour)**	*Compensation Assessment (CPA)*	
		Final Written Exam	

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Objective test	04	One hour	10
2.	Circuit Design test	08	One hour	15
3.	Group Assignment	10	One hour	10
4.	Simulation test	12	One hour	25
	Compensation Assessment (CPA)	16	One hour	10*
5.	Final Written Exam	End of semester	Two hours	40

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings
Anonymous feedback through questionnaire (Mid of the semester & End of the semester)
End semester feedback on Course Outcomes

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, , academic honesty and plagiarism etc.)

MODE OF CORRESPONDENCE (email/ phone etc)

1. All the students are advised to check their NITT WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through their webmail only.
2. Queries (if required) to the course teacher shall only be emailed to digital.eee.nitt@gmail.com

ATTENDANCE

Attendance will be taken by the faculty in all the contact hours.
Attendance Policy is as per Institute norms.

COMPENSATION ASSESSMENT

1. Attending all the assessments are MANDATORY for every student.
2. If any student is not able to attend any of the continuous assessments (CAs* : 1 only) due to genuine reason, student is permitted to attend the compensation assessment (CPA) with % weightage equal to maximum of the CAs. However, maximum of the % weightage among the assessments for which the student was absent will be considered for computing marks for CA.
3. At any case, CPA will not be considered as an improvement test.
4. The minimum marks for passing this course and grading pattern will adhere to the regulations of the Institute.

ACADEMIC HONESTY & PLAGIARISM

1. Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
2. Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
3. The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.
4. The above policy against academic dishonesty shall be applicable for all the programmes.
5. Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

ADDITIONAL INFORMATION

The faculty is available for consultation at times as per the intimation given by the faculty.

Queries may also be emailed to the Course Coordinator directly at digital.eee.nitt@gmail.com

FOR APPROVAL

Course Faculty  **CC-Chairperson**  Pinkymol K.P **HOD** 

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