NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI.

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE PLAN – PART I			
Name of the programme and specialization	**B.Tech. (EEE)**		
Course Title	**VLSI Design**		
Course Code	**EE PE 39**	No. of Credits	**03**
Course Code of Pre-requisite subject(s)		**EEPC15, EEPC17**	
Session	**January 2021**	Section	**A & B**
Name of Faculty	**Dr. S. Moorthi**	Department	**EEE**
Official Email	**srimoorthi@nitt.edu**	Telephone No.	**04312503267**
Course Type	**ELECTIVE course**		

Syllabus (approved in BoS)

MOS characteristics: NMOS characteristics, inverter action – CMOS characteristics, inverter action - models and second order effects of MOS transistors – Current equation – MOSFET Capacitances - MOS as Switch, Diode/ resistor – current source and sink – Current mirror.

CMOS Fabrication – n-well, p-well, twin-tub processes – fabrication steps – crystal growth – photolithography – oxidation – diffusion – Ion implantation – etching – metallization.

CMOS Logic Circuits: Implementation of logic circuits using nMOS and CMOS, Pass transistor and transmission gates – Implementation of combinational circuits – parity generator – magnitude comparator – stick diagram – layout design.

Memory design – SRAM cell – 6T SRAM – DRAM – 1T, 3T, 4T cells, CMOS Sequential circuits: Static and Dynamic circuits – True Single-phase clocked registers – Clocking schemes.

ASIC - Types of ASICs - Design flow – Design Entry – Simulation – Synthesis – Floor planning – Placement – Routing - Circuit extraction – Programmable ASICs.

Text Books:

1. Neil Weste, David Harris, 'CMOS VLSI Design: A Circuits and Systems Perspective', AddisonWesley, 4th Edition, 2010.
2. Debaprasad Das, 'VLSI Design', Oxford University Press, 2010.
3. Ken Martin, 'Digital Integrated Circuits', Oxford University Press, 1999.
4. Peter Van, 'Microchip Fabrication', Mc-Graw Hill Professional, 6th Edition, 2014.

Reference Books:

1. M. J. S. Smith, 'Application Specific Integrated Circuits', Addison Wesley, 1997.
2. Uyemura, 'Introduction to VLSI Circuits and Systems', Wiley, 1st Edition, 2012.

COURSE OBJECTIVES

To enrich the student with the concepts of VLSI devices and its fabrication and also to develop different electronic circuits.

MAPPING OF COs with POs

Course Outcomes	Programme Outcomes (PO)
1. To understand the insights of the MOS devices and its characteristics.	**1-3, 6-10, 12, 13**
2. To appreciate the different VLSI process technologies.	**1-3, 6-10, 12, 13**
3. To design the CMOS combinational logic circuits and its layout.	**1-3, 6-10, 12, 13**
4. To develop the sequential circuits and clocking schemes.	**1-3, 6-10, 12, 13**
5. To realize the Design flow of application-specific Integrated circuit.	**1-3, 6-10, 12, 13**

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COURSE PLAN – PART II

COURSE OVERVIEW

A Course on VLSI Design would benefit the students to enhance their electronics knowledge in the field of large scale integration by the design of both analog and digital circuits effectively and fabrication of integrated circuits which needs the background knowledge of Digital and Linear Integrated Circuits.

COURSE TEACHING AND LEARNING ACTIVITIES (Add more rows)

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1	Week 1, Hour 1	Introduction to VLSI Design and Course plan elaboration	PPT
2	Week 1 to Week 4 Hours 2 – 10	CMOS Logic Circuits-Implementation of logic circuits using nMOS and CMOS, Pass transistor and transmission gates – Implementation of combinational circuits – parity generator – magnitude comparator – stick diagram – layout design.	C&T
3	Week 4 to Week 7 Hours 11 – 19	Memory design – SRAM cell – 6T SRAM – DRAM – 1T, 3T, 4T cells, CMOS Sequential circuits: Static and Dynamic circuits – True Single-phase clocked registers – Clocking schemes.	C&T
4	Week 7 to Week 10 Hours 20 – 28	MOS characteristics: NMOS characteristics, inverter action – CMOS characteristics, inverter action - models and second order effects of MOS transistors – Current equation – MOSFET Capacitances - MOS as Switch, Diode/ resistor – current source and sink – Current mirror.	C&T and PPT
5	Week 10 – Week 13 Hours 29 – 37	CMOS Fabrication – n-well, p-well, twin-tub processes – fabrication steps – crystal growth – photolithography – oxidation – diffusion – Ion implantation – etching – metallization.	PPT and Video
6	Week 13 – Week 16 Hours 38 – 46	ASIC - Types of ASICs - Design flow – Design Entry – Simulation – Synthesis – Floor planning – Placement – Routing - Circuit extraction – Programmable ASICs.	PPT (flipped-class)

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No	Mode of Assessment	Week/Date	Duration	% Weightage
1	Diagnostic Test	Week 2	30 minutes	10
2	Circuit design Assessment	Week 5	60 minutes	20
3	Simulation Group Assignment	Week 10	60 minutes	10
4	Simulation Test	Week 12	60 minutes	20
CPA	Compensation Assessment*	Before end semester	60 minutes	10 (max.)
5	Final Assessment	End semester	120 minutes	40

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedback from the students during class committee meetings.
Anonymous feedback through questionnaire (Mid and end of the semester)
End semester feedback on course outcomes.

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COURSE POLICY (including compensation assessment to be specified**)**

MODE OF CORRESPONDENCE (email/ phone etc)

1. All the students are advised to check their NITT WEBMAIL regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through their webmail only.
2. Queries (if required) to the course teacher shall only be emailed to digital.eee.nitt@gmail.com

ASSESSMENTS:

1. Attending all the assessments are MANDATORY for every student.
2. If any student is not able to attend any of the continuous assessments (CA* : 1 only) due to genuine reason, student is permitted to attend the compensation assessment (CPA) with % weightage equal to maximum of the CAs. However, maximum of the % weightage among the assessments for which the student was absent will be considered for computing marks for CA.
3. At any case, CPA will not be considered as an improvement test.
4. The minimum marks for passing this course and grading pattern will adhere to the regulations of the Institute.

ATTENDANCE POLICY

As per the Institute norms.

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.
- The above policy against academic dishonesty shall be applicable for all the programmes.

FOR APPROVAL

Course Faculty _____ **CC- Chairperson** _____ **HOD** Approved By HOD _____