DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	**B. Tech**		
Course Title	**VLSI SYSTEMS**		
Course Code	**ECPC23**	**No. of Credits**	**3**
Course Code of Pre- requisite subject(s)	**ECPC21**		
Session	**JAN - 2024**	**Section (if, applicable)**	**VI-Sec-B**
Name of Faculty	**Dr. Bukke Chandrababu Naik**	**Department**	**ECE**
Official Email	**chandrababu@nitt.edu**	**Telephone No.**	**7396065605**
Name of course Coordinator(s) (if, applicable)			
Official E-mail		**Telephone No.**	
Course Type (please tick appropriately**)**	☑ **Core course**	☐ **Elective course**	

Syllabus (approved in BoS)

VLSI design methodology, VLSI technology- NMOS, CMOS and BICMOS circuit fabrication. Layout design rules. Stick diagram. Latch up.

Characteristics of MOS and CMOS switches. Implementation of logic circuits using MOS and CMOS technology, multiplexers and memory, MOS transistors, threshold voltage, MOS device design equations. MOS models, small-signal AC analysis. CMOS inverters, propagation delay of inverters, Pseudo NMOS, Dynamic CMOS logic circuits, power dissipation.

Programmable logic devices- antifuse, EPROM and SRAM techniques. Programmable logic cells. Programmable inversion and expander logic. Computation of interconnect delay, Techniques for driving large off-chip capacitors, long lines, Computation of interconnect delaysin FPGAs Implementation of PLD, EPROM, EEPROM, static and dynamic RAM in CMOS.

An overview of the features of advanced FPGAs, IP cores, Softcore processors, Various factors determining the cost of a VLSI, Comparison of ASICs, FPGAs , PDSPs and CBICs . Fault tolerant VLSI architectures

VLSI testing -need for testing, manufacturing test principles, design strategies for test, chiplevel and system level test techniques.

COURSE OBJECTIVES

To introduce various aspects of VLSI circuits and their design including testing.

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Course Outcomes	**Programme Outcomes (PO) (**Enter Numbers only**)**
CO1: Describe the techniques used for VLSI fabrication, design of CMOS logic circuits, switches and memory	**1-L, 3-H, 4-H, 5-M**
CO2: Describe the techniques used the design of CMOS logic circuits,switches and memory in VLSI	**1-M, 3-M, 4-H, 5-H**
CO3: Generalize the design techniques and analyze the characteristics of VLSI circuits such as area, speed and power dissipation	**1-M, 2-M, 3-H, 4-M, 5-M, 7-M, 12-H**
CO4: Explain and compare the architectures for FPGA, PAL and PLDs and evaluate their characteristics such as area, power dissipation and reliability. Use the advanced FPGAs to realize Digital signal processing systems	**1-M, 2-M, 3-H, 4-M, 5-M, 7-M, 12-H**
CO5: Describe the techniques for fault tolerant VLSI circuits. Explain and compare the techniques for chip level and board level testing	**1-M, 2-M, 3-H, 4-M, 5-M, 7-M, 12-H**

COURSE PLAN – PART II

COURSE OVERVIEW

This course provides the knowledge about NMOS, BICMOS and CMOS technologies. Students will be able to learn about Programmable logic devices and cells. They can acquire knowledge about FPGAs Implementation of PLD, EPROM, EEPROM and VLSI testing.

COURSE TEACHING AND LEARNING ACTIVITIES **(Add** more rows)

S.No.	Week/Contct Hours	Topic	Mode of Delivery
1	Week 1	VLSI design methodology, VLSI technology- NMOS, CMOS and BICMOS circuit fabrication.	PPT/board
2	Week 2	Layout design rules. Stick diagram. Latch up. Characteristics of MOS and CMOS switches.	PPT/board
3	Week 3	Implementation of logic circuits using MOS and CMOS technology, multiplexers and memory,	PPT/board
4	Week 4	MOS transistors, threshold voltage, MOS device design equations. MOS models, small-signal AC analysis.	PPT/board
5	Week 5	CMOS inverters, propagation delayof inverters, Pseudo NMOS, Dynamic CMOS logic circuits, power dissipation	PPT/board
6	Week 6	Programmable logic devices-antifuse, EPROM and SRAM techniques. Programmable logic cells	PPT/board

7	Week 7	Programmable inversion and expander logic. Computation of interconnect delay, Techniques for driving large off-chip capacitors, long lines,	PPT/board
8	Week 8	Computation of interconnect delaysin FPGAs Implementation of PLD	PPT/board
9	Week 9	EPROM, EEPROM, static and dynamic RAM in CMOS.	PPT/board
10	Week 10	An overview of the features of advanced FPGAs, IP cores, Soft-core processors	PPT/board
11	Week 11	Various factors determining thecost of a VLSI, Comparison of ASICs, FPGAs , PDSPs and CBICs.	PPT/board
12	Week 12	Fault tolerant VLSI architectures VLSI testing -need for testing	PPT/board
13	Week 13	Manufacturing test principles, design strategies for test,	PPT/board
14	Week 14	Chip level and system level test techniques.	PPT/board

COURSE ASSESSMENT METHODS (shall range from 4 to 6**)**

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	ASSESSMENT I (Cycle Test 1) Descriptive Type Examination 2 Units (Module 1 & 2)	Second week of February	60 minutes	20
2	ASSESSMENT II (Cycle Test II) Descriptive Type Examination 2 Units (Module 3 & 4)	Fourth week of March	60 minutes	20
3	ASSESSMENT III Seminar/Assignment (Module 5)	Third week of April		10
CPA	Compensation Assessment* (Institute Procedure) (Modules1 to 4)		60 minutes	20
4	FINAL ASSESSMENT * (Institute Procedure) Descriptive Type Examination All Modules	Second week of May	180 minutes	50

***mandatory; refer to guidelines on page 3&4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

1. Direct feedback from the students by having face-to-face meeting individually and as the class as a whole.
2. Feedback from the students during the class committee meetings

COURSE POLICY (including compensation assessment to be specified**)**

1. Direct feedback from the students by having face-to-face meeting individually and as the class as a whole.
2. Feedback from the students during the class committee meetings

COURSE POLICY (including compensation assessment to be specified**)**

COMPENSATION ASSESSMENT

- Attending all the assessments is MANDATORY for every student.
- If any student is not able to attend either one or both of the continuous assessments I & II due to genuine reason, student is permitted to attend the compensation assessment (CPA) with only 20 % weightage for both the cases.
- At any case, CPA will not be considered as an improvement test.
- CPA is for only those who cannot attend assessment I or II due to medical emergency and is not applicable for assessment III & IV.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- At least 75% attendance in each course is mandatory.
- A maximum of 10% shall be allowed under On Duty (OD) category.
- Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

ACADEMIC DISHONESTY & PLAGIARISM

- Discussing/talking to other students, sharing material and copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.
- The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION, IF ANY

Students can clarify their doubts by writing to the teacher's email chandrababu@nitt.edu; Detailed discussions can be planned apart from regular classes. The students must come prepared for the discussion with background preparation. Minor doubts will be clarified after the contact hours without any prior appointment through the online platform.

FOR APPROVAL

Course Faculty 19/01/24 **CC- Chairperson** 22-01-24 **HOD** 22/1/2024

(Dr. B. Chandrababu Naik)