**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI**

| COURSE PLAN-PART I | | | |
|---|---|---|---|
| **Course Title** | **Optimizations of Digital Signal Processing Structures for VLSI** | | |
| **Course Code** | **EC663** | **No. of Credits** | **3** |
| **Course Code of Pre-requisite subjects** | **-** | | |
| **Session** | **July - 2023** | **Sem/Section (if, applicable)** | **I Sem. - VLSI System & Communication Systems (M.Tech.)** |
| **Name of Faculty** | **Dr. G Lakshminarayanan** | **Department** | **ECE** |
| **Email** | **laksh@nitt.edu** | **Telephone No.** | **0431-2503307** |
| **Name of Course Coordinator (s) (if, applicable)** | **Dr. G Lakshminarayanan** | | |
| **E-mail** | **laksh@nitt.edu** | **Telephone No.** | **0431-2503307** |
| **Course Type** | ☑ **Elective course** ☐ **Core course** | | |

**Syllabus (approved in BoS)**

An overview of DSP concepts, Pipelining of FIR filters. Parallel processing of FIR filters. Pipelining and parallel processing for low power, Combining Pipelining and Parallel Processing.

Transformation Techniques: Iteration bound, Retiming, Folding and Unfolding.

Pipeline interleaving in digital filters. Pipelining and parallel processing for IIR filters. Low power IIR filter design using pipelining and parallel processing, Pipelined adaptive digital filters.

Algorithms for fast convolution: Cook-Toom Algorithm, Cyclic Convolution. Algorithmic strength reduction in filters and transforms: Parallel FIR Filters, DCT and inverse DCT, Parallel Architectures for Rank-Order Filters.

Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining, Implementation of wave-pipelined systems, Asynchronous pipelining.

**COURSE OBJECTIVES**

- To understand the various VLSI architectures for digital signal processing.
- To know the techniques of critical path and algorithmic strength reduction in the filter
- structures.
- To enable students to design VLSI system with high speed and low power.
- To encourage students to develop a working knowledge of the central ideas of implementation of DSP algorithm with optimized hardware

**COURSE OUTCOMES (CO)**

| Course Outcomes | Aligned Programme Outcomes(PO) |
|---|---|
| **Students will be able** : | |
| ▪ To understand the overview of DSP concepts and design architectures for DSP algorithms and also to perform pipelining and parallel processing on FIR system to achieve high speed and low power. | PO1(L), PO2(M), PO3(H), PO4(H), PO5(H), PO6(H) |
| ▪ To improve the overall performance of DSP system through various transformation and optimization techniques. | |
| ▪ To perform pipelining and parallel processing on IIR system to achieve high speed and low power. | |
| ▪ To optimize design in terms of computation complexity and speed. | |
| ▪ To understand clock based issues and design asynchronous and wave pipelined systems. | |

## COURSE PLAN - PART II

**COURSE OVERVIEW**

This course provides the students to design and develop high performance VLSI DSP architectures. They will be able to understand various transformation techniques like pipelining, parallel processing, retiming. This course also discusses about designing low power FIR and IIR filters which plays a vital role in any signal processing devices. Wave pipelining is introduced in this course along with synchronous and Asynchronous pipelining.

**COURSE TEACHING AND LEARNING ACTIVITIES**

| S. No. | Week | Topic | Mode of Delivery |
|---|---|---|---|
| 1 | 1st Week (3 Contact Hours) | An overview of DSP concepts, Pipelining of FIR filters. Parallel processing of FIR filters | Chalk &Talk, PPT or any suitable mode |
| 2 | 2nd Week (3 Contact Hours) | Pipelining and parallel processing for low power, Combining Pipelining and Parallel Processing | |
| 3 | 3rd Week (3 Contact Hours) | Solving problems, Introduction to Transformation Techniques - Iteration bound | |
| 4 | 4th Week (3 Contact Hours) | Solving problems on Iteration bound, Retiming | |

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|---|---|---|---|
| **5** | **5th Week (3 Contact Hours)** | Solving problems on Retiming, Folding | |
| **6** | **6th Week (3 Contact Hours)** | Unfolding and Solving problems on Folding and Unfolding | |
| **7** | **7th Week** | **Assessment I (60 minutes)** | **Written Exam (Descriptive)** |
| | **(1 Contact Hours)** | Pipeline interleaving in digital filters, Pipelining for IIR filters | Chalk &Talk, PPT or any suitable mode |
| **8** | **8th Week (3 Contact Hours)** | Parallel processing for IIR filters, Low power IIR filter design using pipelining and parallel processing, | |
| **9** | **9th Week (3 Contact Hours)** | Pipelined adaptive digital filters and Solving problems. | |
| **10** | **10th Week (3 Contact Hours)** | Introduction to Algorithms for fast convolution, Cook-Toom Algorithm, Cyclic Convolution. Algorithmic strength reduction in filters and transforms: Parallel FIR Filters. | |
| **11** | **11th Week (3 Contact Hours)** | DCT and inverse DCT, Parallel Architectures for Rank-Order Filters | |
| **12** | **12th Week (1 Contact Hours)** | Solving Problems | |
| | | **Assessment II (60 minutes)** | **Written Exam (Descriptive)** |
| **13** | **13th Week (3 Contact Hours)** | Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs | Chalk &Talk, PPT, Seminar or any suitable mode |
| **14** | **14th Week (3 Contact Hours)** | Wave pipelining, constraint space diagram and degree of wave pipelining, Implementation of wave-pipelined systems. | |
| | | **Compensation Assessment (CPA) (60 minutes)** | **Written Exam (Descriptive)** |
| **15** | **15th Week (2 Contact Hours)** | Asynchronous pipelining, Solving problems | |
| **16** | **16th Week** | **Final Assessment (180 minutes)** | **Descriptive type of exam** |

**COURSE ASSESSMENT METHODS**

| S. No. | Mode of Assessment | Week/Date | Duration | % Weightage |
|---|---|---|---|---|
| 1 | ASSESSMENT-I (Descriptive) | Week 7 | 60 minutes | 20 |

| | | | | |
|---|---|---|---|---|
| 2 | ASSESSMENT-II (Descriptive) | Week 12 | 60 minutes | 20 |
| 3 | Compensation Assessment (CPA) | Week 14 | 60 minutes | 20 (Refer Course Policy) |
| 4 | Assignment/Quiz/Seminar/ Mini Project/MCQs | Between week 8 and week 12 | - | 10 |
| 5 | **Final Assessment (Descriptive type of exam)** | **Week 16** | **180 minutes** | **50** |

**ESSENTIAL READINGS :**

**Text Books:**

1. *K.K.Parhi, VLSI Digital Signal Processing Systems, John-Wiley, 2007*

**Reference Books:**

1. *U. Meyer -Baese, Digital Signal Processing with FPGAs, Springer, 2004*
2. *Wayne Burleson, Konstantinos Konstantinides, Teresa H. Meng, VLSI Signal Processing,1996.*
3. *Richard J. Higgins, Digital signal processing in VLSI, 1990.*
4. *Sun Yuan Kung, Harper J. Whitehouse, VLSI and modern signal processing, 1985*
5. Magdy A. Bayoumi, VLSI Design Methodologies for Digital Signal Processing, 2012
6. *Earl E. Swartzlander, VLSI signal processing systems, 1986*

**COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)**

- Through questionnaire.

Course feedback from the students is obtained at regular intervals and also during class committee meeting.

**COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)**

**MODE OF CORRESPONDENCE (email/phone etc.)**

1. All the students are advised to attend the class regularly.
2. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be intimated in class/ over phone/ in faculty room / through their webmail.

**ASSESSMENT & GRADING POLICY**

1. Attending all the assessments are mandatory.
2. Schedule for all the assessments will be intimated in class or through class committee meeting.
3. Those who are unable to attend either of the assessment I & II under medical reasons are allowed to appear for CPA (Compensation Assessment) with 20% weightage. Portion for CPA is both Assessment I & Assessment II Portions.
4. At any case, CPA will not be considered as an improvement test.
5. Institute regulations will be followed for fixing minimum passing marks, grading pattern, Reassessment, FA, and Redo.

**ATTENDANCE POLICY** (A uniform attendance policy as specified below shall be followed)

1. **At least 75% attendance in each course is mandatory.**
2. **A maximum of 10% shall be allowed under On Duty (OD) category.**
3. Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.**

**ACADEMIC DISHONESTY & PLAGIARISM**

1. Possessing a mobile phone, carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
2. Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
3. The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

   The above policy against academic dishonesty shall be applicable for all the programmes.

**ADDITIONAL INFORMATION**

Queries and feedback may also be emailed to the Course Faculty directly at laksh@nitt.edu

**FOR APPROVAL**

**Course Faculty** _____ (G.LAKSHMINARAYANAN)
**Date: 28.08.2023**

**CC-Chairperson** R. Thilagavathy 31.08.2023

**HOD** _____

**Guidelines:**

a) The number of assessments for a course shall range from 4 to 6.

b) Every course shall have a final assessment on the entire syllabus with at least 30% weightage.

c) One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered.

d) The passing minimum shall be as per the regulations. Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.

e) Absolute grading policy shall be incorporated if the number of students per course is less than 10.

f) Necessary care shall be taken to ensure that the course plan is reasonable and is objective.