DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Name of the programme and specialization	**BACHELOR OF TECHNOLOGY ELECTRONICS AND COMMUNICATION ENGINEERING**		
Course Title	**MICROPROCESSORS AND MICROCONTROLLERS**		
Course Code	**ECPE12**	**No. of Credits**	**3**
Course Code of Pre-requisite subject(s)	**ECPC14 DIGITAL CIRCUITS AND SYSTEMS**		
Session	**January 2023**	**Section (if, applicable)**	**B**
Name of Faculty	**Dr. Srinivasulu Jogi**	**Department**	**ECE**
Email	**srinivasulu@nitt.edu**	**Telephone No.**	**8248835354**
Name of Course Coordinator(s) (if, applicable)			
E-mail		**Telephone No.**	
Course Type	☐ **Core course** ☑ **Elective course**		

Syllabus (approved in BoS)

Microprocessor based personal computer system. Software model of 8086. Segmented memory operation. Instruction set. Addressing modes. Assembly language programming. Interrupts. Programming with DOS and BIOS function calls.

Hardware detail of 8086. . Bus timing. Minimum vs Maximum mode of operation. Memory interface. Parallel and serial data transfer methods. 8255 PPI chip. 8259 Interrupt controller. 8237 DMA controller.

Microcontroller. Von-Neumann Vs Harvard architecture. Programming model. Instruction set of 8051 Microcontroller. Addressing modes. Programming. Timer operation.

Mixed Signal Microcontroller: MSP430 series. Block diagram. Address space. On-chip peripherals -analog and digital. Register sets. Addressing Modes. Instruction set. Programming. FRAM vs flash for low power and reliability.

Peripheral Interfacing using 8051 and Mixed signal microcontroller. Serial data transfer -UART, SPI and I2C. Interrupts. I/O ports and port expansion. DAC, ADC, PWM, DC motor, Stepper motor and LCD interfacing.

Text Books:

- James L. Antonakos, “An Introduction to the Intel Family of Microprocessors”, Pearson, 1999

- M.A.Mazidi&J.C.Mazidi "Microcontroller and Embedded systems using Assembly & C. (2/e)", Pearson Education, 2007.
- John H. Davies, "MSP430 Microcontroller Basics", Elsevier Ltd., 2008
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Reference Books:

- Barry B. Brey, "The Intel Microprocessors", (7/e), Eastern Economy Edition , 2006.
- K.J. Ayala, "The 8051 Microcontroller ", (3/e), Thomson Delmar Learning, 2004.
- I. S. MacKenzieand R.C.W.Phan., " The 8051 Microcontroller.(4/e)", Pearson education, 2008.

COURSE OBJECTIVES

This subject deals about the basics of 16-bit Microprocessor, 8-bit and 16-bit Micro controllers, their architectures, internal organization and their functions, peripherals, and interfacing.

COURSE OUTCOMES (CO)

Course Outcomes	**Aligned Programme Outcomes (PO)**
After successful completion of the course the students are able to	
CO1: Recall and apply the basic concept of digital Fundamentals to Microprocessor based personal computer system.	PO1,PO5,PO8,PO9, PO11, PO12, PSO1-H PO2,PO3,PO4-L
CO2: Illustrate how the different peripherals are interfaced with Microprocessor.	PO1,PO8, PSO1-H PO2,PO3,PO4,PO5, PO9,PO11-M PO12-L
CO3: Distinguish and analyze the properties of Microprocessors & Microcontrollers.	PO8, PSO1-H PO1,PO2,PO3,PO4, PO5,PO9,PO11-M PO12, PSO3-L
CO4: Understand a low power and reliability concept of mixed signal Microcontrollers.	PO1,PO5,PO8,PO12-H PO9,PO11, PSO2-M PO2,PO3,PO4, PSO3-L
CO5: Analyze the data transfer information through serial & parallel ports.	PO3,PO4,PO5,PO8, PO9,PO11,PO12-H PO1,PO2, PSO2-M PO6,PO7,PO10-L
	H-High-3 M- Medium-2 L-Low-1

COURSE PLAN – PART II

COURSE OVERVIEW

This course provides a short introduction to embedded electronic systems, where they are used, and ways in which they can be implemented. Microcontrollers were originally developed from Microprocessors for use in embedded electronic control systems, as their name implies. They include a processor and most or all of the memory, clock, and other systems nedded to support it. Everything is inside a single package.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	**Week/Contact Hours**	**Topic**	**Mode of Delivery**
1	Third week of January	Microprocessor based personal computer system. Software model of 8086.	Chalk & Talk, PPT

2	Fourth week of January	Segmented memory operation. Instruction set. Addressing modes.	Chalk & Talk, PPT
3	First week of February	Assembly language programming. Interrupts.	Chalk & Talk, PPT
4	Second week of February	Programming with DOS and BIOS function calls	PPT
5	Third week of February	Hardware detail of 8086. Bus timing. Minimum vs Maximum mode of operation.	Chalk & Talk, PPT
6	Fourth week of February	Memory interface. Parallel and serial data transfer methods	Chalk & Talk, PPT
7	First week of March	8259 Interrupt controller. 8237 DMA controller	PPT
8	Second week of March	Von-Neumann Vs Harvard architecture. Programming model - 8051	Chalk & Talk, PPT
9	Third week of March	Instruction set of 8051 Microcontroller. Addressing modes. Programming. Timer operation.	Chalk & Talk, PPT
10	Fourth week of March	Mixed Signal Microcontroller: MSP430 series. Block diagram. Address space.	Chalk & Talk, PPT
11	First week of April	Serial data transfer - UART, SPI and I2C.	PPT
12	Second week of April	Interrupts. I/O ports and port expansion	Chalk & Talk, PPT
13	Third week of April	DAC, ADC, LCD, DC motor and Stepper motor interfacing with Microcontroller.	PPT
14	Fourth week of April	PWM generation and peripheral interfacing with MSP430	PPT

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assessment -1 Assignment 1	February second week		5 marks (1st unit)
2	Assessment -2 (Descriptive type exam)	February last week	1 Hour	20 marks (2 units) Unit 1 & 2
3	Assessment -3 (Descriptive type exam)	March last week	1 Hour	20 marks (2 units) Unit 3 & 5
4	Assessment -4 Assignment 2	April second week		5 marks (5 th unit)
CPA	Compensation Assessment*	April last week (If applicable)	1 Hour	20 marks (1,2,3 & 5 units)
5	Assessment – 5 * (Descriptive type exam) End semester exam	May second week	3 Hours	50 marks (All 5 units)

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Course feedback is assessed through

1. Class committee meeting
2. Frequently ask the questions in the class and analyzes the responses
3. Course exit survey form

Course Attainment is calculated through

Direct tools (Exams and Assignments)

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

COURSE ASSESSMENT:

1 Attending all the assessments are MANDATORY for every student.
2 Assignment submission is MANDATORY for every student within the stipulated time failing which 10% weightage will not be considered for final grade assessment.
3 There will not be any improvement test for the students who score low marks in continuous assessment test.
4 Finally, every student is expected to score minimum marks as per the regulations of the institute out of the total assessments 1,2,3,4 and 5 to pass the course. Otherwise the student will be declared fail and 'F' grade will be awarded. Further the student can take up only FORMATIVE ASSESSMENT.

MODE OF CORRESPONDENCE (email/ phone etc.)

1 All students are advised to check their NITT webmail account regularly. All the details about the schedule of classes, schedule of assessments, course material and any other information regarding the course will be sent through webmail only.
2 Doubts regarding the course can be clarified through webmail and in the concerned class hours.
3 Queries, if any regarding the course shall through email to the Faculty and in the concerned class hours.

COMPENSATION ASSESSMENT POLICY

1 Any student who fails to maintain 75% attendance only on reasonable medical/official grounds needs to appear for the compensation assessment (CPA) classes.
2 The portion for compensation assessment will be the portion of assessment 2 and 3. There is no CPA for Assessment 1 and 4.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- **At least 75% attendance in each course is mandatory.**
- **A maximum of 10% shall be allowed under On Duty (OD) category.**
- Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.**

ACADEMIC DISHONESTY & PLAGIARISM

1. Sharing the answers through electronic media or any other mode will be treated as dishonesty and it is punishable.
2. Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.

3. The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

Any queries send a mail to srinivasulu@nitt.edu

FOR APPROVAL

Course Faculty _____ **CC-Chairperson** _____ **HOD** _____