

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION  
ENGINEERING**

<b>COURSE PLAN – PART I</b>			
<b>Name of the programme and specialization</b>	<b>M.Tech VLSI SYSTEM</b>		
<b>Course Title</b>	<b>DIGITAL SYSTEM DESIGN</b>		
<b>Course Code</b>	<b>EC661</b>	<b>No. of Credits</b>	<b>3</b>
<b>Course Code of Pre-requisite subject(s)</b>			
<b>Session</b>	<b>JULY 2022</b>	<b>Section (if, applicable)</b>	
<b>Name of Faculty</b>	<b>Mr. Naresh V</b>	<b>Department</b>	<b>ECE</b>
<b>Official Email</b>	<b>jmr.naresh@gamil.com</b>	<b>Telephone No.</b>	<b>9618857966</b>
<b>Name of Course Coordinator(s) (if, applicable)</b>			
<b>Official E-mail</b>		<b>Telephone No.</b>	
<b>Course Type</b> (please tick appropriately)	<b>Elective course</b>		
<b>Syllabus (approved in BoS)</b>			
<p>Mapping algorithms into Architectures: Data path synthesis, control structures, critical path and worst-case timing analysis. FSM and Hazards.</p> <p>Combinational network delay. Power and energy optimization in combinational logic circuit. Sequential machine design styles. Rules for clocking. Performance analysis.</p> <p>Sequencing static circuits. Circuit design of latches and flip-flops. Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.</p> <p>Data path and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context addressable memory.</p> <p>Reconfigurable Computing- Fine grain and Coarse grain architectures, Configuration architectures Single context, Multi context, partially reconfigurable, Pipeline reconfigurable, Block Configurable, Parallel processing</p>			
<b>COURSE OBJECTIVES</b>			
To get an idea about designing complex, high speed digital systems and how to implement such design.			
<b>MAPPING OF COs with POs</b>			

<b>Course Outcomes</b>	<b>Programme Outcomes (PO) (Enter Numbers only)</b>
CO1: identify mapping algorithms into architectures.	<b>1-L, 2-H, 3-H, 4-M</b>
CO2: summarize various delays in combinational circuit and its optimization methods.	<b>2-M, 3-H, 5-H, 4-M</b>
CO3: summarize circuit design of latches and flip-flops.	<b>2-M, 5-H, 6-H</b>
CO4: construct combinational and sequential circuits of medium complexity that is based on VLSIs, and programmable logic devices.	<b>1-H, 2-H, 5-H</b>
CO5: summarize the advanced topics such as reconfigurable computing, partially reconfigurable, Pipeline reconfigurable architectures and block configurable.	<b>3-H, 4-H, 6-H</b>

<b>COURSE PLAN – PART II</b>			
<b>COURSE OVERVIEW</b>			
To get an idea about designing complex, high speed digital systems and how to implement such design			
<b>COURSE TEACHING AND LEARNING ACTIVITIES</b>			<b>(Add more rows)</b>
<b>S.No.</b>	<b>Week/Contact Hours</b>	<b>Topic</b>	<b>Mode of Delivery</b>
1	1 <sup>st</sup>	Mapping algorithms into Architectures: Data path synthesis, control structures,	PPT/board
2	2 <sup>nd</sup>	critical path and worst case timing analysis	PPT/board
3	3 <sup>rd</sup>	FSM and Hazards	PPT/board
4	4 <sup>th</sup>	Combinational network delay. Power and energy optimization in combinational logic circuit.	PPT/board
5	5 <sup>th</sup>	. Sequential machine design styles. Rules for clocking, Performance analysis.	PPT/board
6	6 <sup>th</sup>	Sequencing static circuits. Circuit design of latches and flip-flops	PPT/board
7	7 <sup>th</sup>	Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.	PPT/board
8	8 <sup>th</sup>	Data path and array subsystems: Addition / Subtraction, Comparators	PPT/board
9	9 <sup>th</sup>	counters, coding, multiplication and division	PPT/board
10	10 <sup>th</sup>	SRAM, DRAM, ROM, serial access memory, context addressable memory.	PPT/board
11	11 <sup>th</sup>	Reconfigurable Computing- Fine grain and Coarse grain architectures, Configuration architectures Single context, Multi context, partially reconfigurable	PPT/board
12	12 <sup>th</sup>	Pipeline reconfigurable, Block Configurable, Parallel processing	PPT/board

<b>COURSE ASSESSMENT METHODS</b> (shall range from 4 to 6)				
<b>S.No.</b>	<b>Mode of Assessment</b>	<b>Week/Date</b>	<b>Duration</b>	<b>% Weightage</b>
1	ASSESSMENT I (Cycle Test 1) Descriptive Type Examination 2 Units	Second week of October	60 minutes	20
2	ASSESSMENT II Seminar/Assignment	First week of November		10
3	ASSESSMENT III (Cycle Test II) Descriptive Type Examination 2 Units	Third week of November	60 minutes	20
CPA	Compensation Assessment* (Institute Procedure)		60 minutes	20
4	FINAL ASSESSMENT * (Institute Procedure)	Third week of December	180 minutes	50
<b>*mandatory; refer to guidelines on page 3&amp;4</b>				
<b>COURSE EXIT SURVEY</b> (mention the ways in which the feedback about the course shall be assessed)				
<ol style="list-style-type: none"> <li>1. Direct feedback from the students by having face-to-face meeting individually and as the class as a whole.</li> <li>2. Feedback from the students during the class committee meetings</li> </ol>				
<b>COURSE POLICY</b> (including compensation assessment to be specified)				
<b><u>COMPENSATION ASSESSMENT</u></b>				
<ul style="list-style-type: none"> <li>➤ Attending all the assessments is MANDATORY for every student.</li> <li>➤ If any student is not able to attend either one or both of the continuous assessments I &amp; II due to genuine reason, student is permitted to attend the compensation assessment (CPA) with only 20 % weightage for both the cases.</li> <li>➤ At any case, CPA will not be considered as an improvement test.</li> </ul>				
<b><u>ATTENDANCE POLICY</u></b> (A uniform attendance policy as specified below shall be followed)				
<ul style="list-style-type: none"> <li>➤ At least 75% attendance in each course is mandatory.</li> <li>➤ A maximum of 10% shall be allowed under On Duty (OD) category.</li> <li>➤ Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.</li> </ul>				

### **ACADEMIC DISHONESTY & PLAGIARISM**

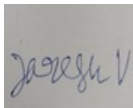
- Discussing/talking to other students, sharing material and copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.
- The above policy against academic dishonesty shall be applicable for all the programmes.

### **ADDITIONAL INFORMATION, IF ANY**

Students can clarify their doubts by writing to the teacher's email [jmr.naresh@gmail.com](mailto:jmr.naresh@gmail.com); Detailed discussions can be planned apart from regular classes. The students must come prepared for the discussion with background preparation. Minor doubts will be clarified after the contact hours without any prior appointment through the online platform.

### **FOR APPROVAL**

Course Faculty



CC- Chairperson



HOD