NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

This course outline template acts as a guide for writing your course outline. As every course is different, please feel free to amend the template/ format to suit your requirements.

COURSE OUTLINE TEMPLATE			
Course Title	HDL Programming Laboratory		
Course Code	EC655	No. of Credits	2
Department	ECE	Faculty	Dr. R. K. Kavitha
Pre-requisites Course Code	None		
Course Coordinator(s) (if, applicable)			
Other Course Teacher(s)/Tutor(s) E-mail	rkkavitha@nitt.edu	Telephone No.	0431-2503322
Course Type	☑ Lab course	☐ Elective course	

COURSE OVERVIEW

This course will Introduce Fundamentals of HDL programming

COURSE OBJECTIVES

- To design combinational, sequential circuits using Verilog HDL.
- To verify and design the digital circuit by means of Computer Aided Engineering tools which involves in programming with the help of Verilog HDL.

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)
After successful completion of the course the students are able to	
CO1: understand the basic concepts of verilog HDL	PO1,2,3 -H PO4,5-M PO6-L
CO2: model digital systems in verilog HDL at different levels of abstraction	PO1,2,3 -H PO4,5-M PO6-L
CO3: know the simulation techniques and test bench creation.	PO1,2,3 -H PO4,5-M PO6-L
CO4: understand the design flow from simulation to synthesizable version	PO1,2,3 -H PO4,5-M PO6-L
CO5: get an idea of the process of synthesis and post-synthesis	PO1,2,3 -H PO4,5-M PO6-L
	H-High M- Medium L=Low

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week	Topic	Mode of Delivery
1.	2nd week of September	Lab course Introduction and Tool Flow Demo	Through weekly Lab experiments
2.	3rd & 4th week of September	Adder/ Subtractor	
3.	First week of October	Multiplexer/ Demultiplexer	
4.	Second week of October	Encoder/ Priority Encoder	
5.	Third week of October	Code Converter	
6.	Fourth week of October	Flipflop	
7.	First week of November	Shift Register/ Universal Shift Register	
8.	Second week of November	Comparator, Upcounter/ Downcounter	
9.	Third week of November	Udps	
10.	Fourth week of November	Memory – ROM, RAM	
11.	First week of December	Array Multiplier/ Array Multiplier With Pipelining	
12.	2nd week of December	FIR Filter/ Fir Filter With Pipelinig	
13.	3rd week of December	Project Demo	

COURSE ASSESSMENT METHODS

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1.	Continuous Assessment			20 marks
2.	Written test (Assessment 1)	December First week	1 Hour	30 marks
3.	Mini Project	December second week	1 Hour	20 marks
4.	End Sem Exam	As per the Academic Calender	3 Hours	30 marks
	Compensation Assesssment	Not Applicable for Labs	-	-

ESSENTIAL READINGS : Textbooks, reference books Website addresses, journals, etc

Text Books:

- 1. M.D.Ciletti, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", PHI, 1999.
- 2. S. Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", Pearson, 2003.

Reference Books:

- *J Bhaskar, "A Verilog HDL Primer (3rd edition)", Kluwer, 2005.*
- *M.G.Arnold, "Verilog Digital – Computer Design", Prentice Hall (PTR), 1999.*
- *Recent literature in Modeling and Synthesis with Verilog HDL.*

COURSE EXIT SURVEY (mention the ways in which the feedback about the course is assessed and indicate the attainment also)

Course feedback is assessed through

1. Class committee meeting
2. Performance in the assessments
3. Course exit survey form

Course Attainment is calculated through

1. Direct tools (Exams and seminars)

COURSE POLICY (including plagiarism, academic honesty, attendance, etc.)

1. The students through class representative may give their feedback at any time which will be duly addressed.
2. Feedback from the students through MIS and class committee meetings.

ADDITIONAL COURSE INFORMATION

Any queries send a mail to rkkavitha@nitt.edu

FOR SENATE'S CONSIDERATION

Course Faculty _____ **CC-Chairperson** _____ **HOD** _____