DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Course Title	**Design of ASICs**		
Course Code	**EC656**	**No. of Credits**	**3**
Course Code of Pre-requisite subject(s)	**--**		
Session	**Jan. 2022**	**Sem/Section (if, applicable)**	**I year - M.Tech. (VLSI System & Communication Systems) & B.Tech (Honours)**
Name of Faculty	**Dr G.Lakshminarayanan**	**Department**	**ECE**
Email	**laksh@nitt.edu**	**Telephone No.**	**0431-2503307**
Name of Course Coordinator(s) (if, applicable)	**Dr G.Lakshminarayanan**		
E-mail	**laksh@nitt.edu**	**Telephone No.**	**0431-2503307/ 9442940144**
Course Type	✓ **Core course**	☐ **Elective course**	

Syllabus (approved in BoS)

Introduction to Technology, Types of ASICs, VLSI Design flow, Design and Layout Rules, Programmable ASICs - Antifuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects. Advanced FPGAs and CPLDs and Soft-core processors. Self-Study: Multi-core processors, High performance computing (HPC), Cache, High speed memories (DDR4), High speed serdes (56Gbps, PAM4), GPU

ASIC physical design issues, System Partitioning, Floorplanning and Placement. Algorithms: K-L, FM, Simulated annealing algorithms. Full Custom Design: Basics, Needs & Applications. Schematic and layout basics, Full Custom Design Flow.

Semicustom Approach: Synthesis (RTL to GATE netlist) - Introduction to Constraints (SDC), Introduction to Static Timing Analysis (STA). Place and Route (Logical to Physical Implementation): Floorplan and Power-Plan, Placement, Clock Tree Synthesis (clock planning), Routing, Timing Optimization, GDS generation.

Overview of Extraction, Logical equivalence and STA: Parasitic Extraction Flow, STA: Timing Flow, LEC: Introduction, flow and Tools used. Physical Verification: Introduction, DRC, LVS and basics of DFM. High performance algorithms for ASICs/ SoCs as case study – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. **Case study:** FSM design, clock domain crossing, FIFOs. Core (ARM) and IOs(I2C, PWM, GPIO, SPI, NAND, Ethernet, USB, high speed serdes etc. are interconnected through AXI/APB buses (protocols and interconnects)

Text Books:

1. *M.J.S. Smith : Application Specific Integrated Circuits, Pearson, 2003*
2. *Sudeep Pasricha and NikilDutt, On-Chip Communication Architectures System on Chip Interconnect, Elsevier, 2008*

Reference Books:

1. *H.Gerez, Algorithms for VLSI Design Automation, John Wiley, 1999*
2. *Jan.M.Rabaey et al, Digital Integrated Circuit Design Perspective (2/e), PHI 2003*
3. *David A.Hodges, Analysis and Design of Digital Integrated Circuits (3/e), MGH 2004*
4. *Hoi-Jun Yoo, Kangmin Leeand Jun Kyong Kim, Low-Power NoC for High-Performance SoC Design, CRC Press, 2008*
5. *An Integrated Formal Verification solution DSM sign-off market trends, www.cadence.com.*

COURSE OBJECTIVES

- To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
- To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.
- To give the student an understanding of High performance algorithms
- To give the student an understanding of System on Chip design including case study

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)
1. Students able to demonstrate VLSI tool-flow and appreciate FPGA and CPLD architectures	PO1,PO2,PO9
2. To be able to understand the issues involved in ASIC design, including technology choice, design management and tool-flow.	PO1,PO2,PO3, PO9
3. Student will be able to understand the algorithms used for ASIC construction and Full Custom Design Flow and Tool used	PO3,PO4,PO5
4. To be able to understand Semicustom Design Flow and Tool used - from RTL to GDS and Logical to Physical Implementation.	PO3,PO4,PO5
5. Student will be able to understand about STA, LEC, DRC, LVS, DFM and appreciate high performance algorithms for ASICs	PO1,PO2,PO3,PO4,PO5
6. To be able to understand the System on Chip and On chip communication architectures and carryout case studies.	PO2,PO3,PO4,PO5

COURSE PLAN – PART II

COURSE OVERVIEW

This course enables the students to understand the task and algorithms running in the backend of every VLSI tools. It also enables to students to know the research areas in the back end of VLSI design and SoC.

COURSE DESCRIPTION :

COURSE TEACHING AND LEARNING ACTIVITIES

Sl. No.	Week/Contact Hours	Topic	Mode of Delivery
1.	Week 1 3 Contact Hours	Introduction to Technology, Types of ASICs, VLSI Design flow, Design and Layout Rules	Lecture C&T/ PPT
2.	Week 2 3 Contact Hours	Programmable ASICs - Antifuse, SRAM, EPROM, EEPROM based ASICs, Programmable ASIC logic cells	
3.	Week 3 3 Contact Hours	Programmable ASIC logic cells – Continued, Programmable I/O cells	
4.	Week 4 3 Contact Hours	Programmable interconnects, Advanced FPGAs and CPLDs and Soft-core processors, ASIC physical design issues.	
5.	Week 5 3 Contact Hours	System Partitioning, Floorplanning and Placement, Algorithms: K-L, FM, Simulated annealing algorithms.	
6.	Week 6 2 Contact Hours	Full Custom Design: Basics, Needs & Applications. Schematic and layout basics, Full Custom Design Flow.	
	ASSESSMENT I		**Written Exam (Descriptive)**

7.	Week 7 3 Contact Hours	Semicustom Approach: Synthesis (RTL to GATE net list), Introduction to Constraints (SDC), Introduction to Static Timing Analysis (STA).	Lecture C&T/ PPT
8.	Week 8 3 Contact Hours	Place and Route (Logical to Physical Implementation): Floorplan and Power-Plan, Placement, Clock Tree Synthesis (clock planning), Routing, Timing Optimization, GDS generation.	
9.	Week 9 3 Contact Hours	Overview of Extraction, Logical equivalence and STA: Parasitic Extraction Flow, STA: Timing Flow, LEC: Introduction, flow and Tools used. Physical Verification: Introduction, DRC, LVS and basics of DFM.	
10.	Week 10 2 Contact Hours	Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.	
	ASSESSMENT II		**Written Exam (Descriptive)**
11.	Week 11 3 Contact Hours	Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures.	Lecture C&T/ PPT
12.	Week 12 3ContactHours	**ASSESSMENT-III** **(**Assignment/Quiz/Seminar/ Mini Project**)**	
13.	Week 13 3 Contact Hours		
14.	Week 14 3 Contact Hours	**Case study:** FSM design, clock domain crossing, FIFOs. Core (ARM) and IOs(I2C, PWM, GPIO	
15.	Week 15 3 Contact Hours	SPI, NAND, Ethernet, USB, high speed serdes etc. are interconnected through AXI/APB buses (protocols and interconnects)	
16.	Week 16 3 Contact Hours	**Compensation Assessment**	**Written Exam (Descriptive)**
17.	Week 17 3 Contact Hours	**Final Assessment**	**Written Exam (Descriptive)**

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

Sl. No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assessment I (Descriptive)	4th week of February 2019	60 Minutes	25
2	Assessment II (Descriptive)	4th week of March 2019	60 Minutes	25
3	Assessment III (either seminar or Assignments or Quiz or Mini project)	2nd week of April 2019	--	20
4	CPA Compensation Assessment	1st week of May 2019	60 Minutes	25 (Refer course policy)
5	Final Assessment (Descriptive)	2nd week of May 2019	120 Minutes	30

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

- Through questionnaire.

Course feedback from the students is obtained at regular intervals and also during class committee meeting.

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)

MODE OF CORRESPONDENCE (email/phone etc.)

1. All the students are advised to attend the classes regularly.
2. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be intimated in class/ over phone/ in faculty room / through their webmail.

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COMPENSATION ASSESSMENT POLICY

1. Attending all the assessments are mandatory.
2. Schedule for all the assessments will be intimated in class or through class committee meeting.
3. Those who are unable to attend either of the assessment I & II under medical reasons are allowed to appear for CPA (Compensation Assessment) with 25% weightage.
4. At any case, CPA will not be considered as an improvement test.
5. Institute regulations will be followed for fixing minimum passing marks, grading pattern, Reassessment, FA, and Redo.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

1. **At least 75% attendance in each course is mandatory.**
2. **A maximum of 10% shall be allowed under On Duty (OD) category.**
3. Students with **less than 65% of attendance** shall be prevented from writing the final assessment and **shall be awarded 'V' grade.**

ACADEMIC DISHONESTY & PLAGIARISM

1. Possessing a mobile phone, keeping bits of paper, talking to other students, copying from others during assessment will be treated as punishable dishonesty.
2. Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
3. The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.

The above policy against academic dishonesty shall be applicable for all the programmes.

ADDITIONAL INFORMATION

Queries and feedback may also be emailed to the Course Faculty directly at laksh@nitt.edu

FOR APPROVAL

Course Faculty _____ **CC-Chairperson** _____ **HOD** _____

(Dr.V.Sudha)

Date: 21.01.2022

Guidelines:

a) The number of assessments for a course shall range from 4 to 6.

b) Every course shall have a final assessment on the entire syllabus with at least 30% weightage.

c) One compensation assessment for absentees in assessments (other than final assessment) is mandatory. Only genuine cases of absence shall be considered.

d) The passing minimum shall be as per the regulations. Attendance policy and the policy on academic dishonesty & plagiarism by students are uniform for all the courses.

e) Absolute grading policy shall be incorporated if the number of students per course is less than 10.

f) Necessary care shall be taken to ensure that the course plan is reasonable and is objective.