DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Course Title	**VLSI SYSTEMS**		
Course Code	**ECPC23**	**No. of Credits**	**3**
Course Code of Pre-requisite subject(s)	**ECPC21**		
Session	**Jan - 2022**	**Section (if, applicable)**	**B**
Name of Faculty	**Dr. R.K.Kavitha**	**Department**	**Electronics and communication engineering**
Email	**rkkavitha@nitt.edu**	**Telephone No.**	**0431-2503322**
Name of Course Coordinator(s) (if, applicable)	**-**		
E-mail	**-**	**Telephone No.**	
Course Type	☑ **Core course**	☐ **Elective course**	

Syllabus (approved in BoS)

VLSI design methodology, VLSI technology- NMOS, CMOS and BICMOS circuit fabrication. Layout design rules. Stick diagram. Latch up.

Characteristics of MOS and CMOS switches. Implementation of logic circuits using MOS and CMOS technology, multiplexers and memory, MOS transistors, threshold voltage, MOS device design equations. MOS models, small-signal AC analysis. CMOS inverters, propagation delay of inverters, Pseudo NMOS, Dynamic CMOS logic circuits, power dissipation.

Programmable logic devices- antifuse, EPROM and SRAM techniques. Programmable logic cells. Programmable inversion and expander logic. Computation of interconnect delay, Techniques for driving large off-chip capacitors, long lines, Computation of interconnect delays in FPGAs Implementation of PLD, EPROM, EEPROM, static and dynamic RAM in CMOS.

An overview of the features of advanced FPGAs, IP cores, Softcore processors, Various factors determining the cost of a VLSI, Comparison of ASICs, FPGAs, PDSPs and CBICs. Fault tolerant VLSI architectures

VLSI testing -need for testing, manufacturing test principles, design strategies for test, chip level and system level test techniques.

COURSE OBJECTIVES

To introduce various aspects of VLSI circuits and their design including testing.

COURSE OUTCOMES (CO)

Course Outcomes	**Aligned Programme Outcomes (PO)**
1. Describe the techniques used for VLSI fabrication, design of CMOS	**PO1, PO3, PO4, PO5**

logic circuits, switches and memory	
2. Describe the techniques used the design of CMOS logic circuits, switches and memory in VLSI	**PO1, PO3, PO4, PO5**
3. Generalize the design techniques and analyze the characteristics of VLSI circuits such as area, speed and power dissipation	**PO1, PO2, PO3, PO4, PO5,PO7, PO12**
4. Explain and compare the architectures for FPGA, PAL and PLDs and evaluate their characteristics such as area, power dissipation and reliability. Use the advanced FPGAs to realize Digital signal processing systems	**PO1, PO2, PO3, PO4, PO5,PO7, PO12**
5. Describe the techniques for fault tolerant VLSI circuits. Explain and compare the techniques for chip level and board level testing	**PO1, PO2, PO3, PO4, PO5,PO7, PO12**

COURSE PLAN – PART II

COURSE OVERVIEW

This course provides the knowledge about NMOS, BICMOS and CMOS technologies. Students will be able to learn about Programmable logic devices and cells. They can acquire knowledge about FPGAs Implementation of PLD, EPROM, EEPROM and VLSI testing.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of Delivery
1	Week 1 (3 contact Hours)	VLSI design methodology, VLSI technology- NMOS, CMOS and BICMOS circuit fabrication.	**Lecture C&T/ PPT or any suitable mode**
2	Week 2 (3 contact Hours)	Layout design rules. Stick diagram. Latch up. Characteristics of MOS and CMOS switches.	
3	Week 3 (3 contact Hours)	Implementation of logic circuits using MOS and CMOS technology, multiplexers and memory,	
4	Week 4 (3 contact Hours)	MOS transistors, threshold voltage, MOS device design equations. MOS models, small-signal AC analysis.	
5	Week5	**ASSESSMENT I - 20Marks**	**Descriptive/Numerial (Written)**
6	Week 6 (3 contact Hours)	CMOS inverters, propagation delay of inverters, Pseudo NMOS, Dynamic CMOS logic circuits, power dissipation	**Lecture C&T/ PPT or any suitable mode**
7	Week 7 (2 contact Hours)	Programmable logic devices- antifuse, EPROM and SRAM techniques. Programmable logic Cells.	

8	Week 7 (1 contact hour)	**ASSESSMENT II - 15 Mark**	**Quiz**
9	Week 8 (3 contact Hours)	Programmable inversion and expander logic. Computation of interconnect delay, Techniques for driving large off-chip capacitors, long lines,	**Lecture C&T/ PPT or any suitable mode**
10	Week 9	**ASSESSMENT III - 20 Marks**	**Descriptive/Numerical (Written)**
11	Week 10 (3 contact Hours)	Computation of interconnect delays in FPGAs Implementation of PLD	**Lecture C&T/ PPT or any suitable mode**
12	Week 11 (3 contact Hours)	EPROM, EEPROM, static and dynamic RAM in CMOS.	
13	Week 12 (3 contact Hours)	An overview of the features of advanced FPGAs, IP cores, Soft-core processors	
14	Week 13 (3 contact Hours)	Various factors determining the cost of a VLSI, Comparison of ASICs, FPGAs , PDSPs and CBICs .	
15	Week 14 (3 contact Hours)	Fault tolerant VLSI architectures VLSI testing -need for testing ,manufacturing test principles, design strategies for test, chip level and system level test techniques.	
16	Week 15	**ASSESSMENT IV - 15 Marks**	**Mini Project**
17	Week 16	**END ASSESSMENT – 30 Marks**	**Descriptive/Numerical (Written)**

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Assessment I	3rd week Feb	(60 minutes)	20 marks
2	Assessment II (Quiz)	2nd Week Mar	(60 minutes)	15 marks
3	Assessment III	3rd Week of March	(60 minutes)	20 marks
4	Assessment IV (Mini Project)	3rd Week of April	(60 minutes)	15 marks

CPA	Assessment V (CPA)	3rd Week of April	(60 minutes)	20 marks
6	End Assessment	4th Week of April	(180 minutes)	30 marks

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

1. Feedback from the students during class committee meeting.
2. Queries through questionnaire.

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, academic honesty and plagiarism etc.)

MODE OF CORRESPONDENCE (email/ phone etc)

1. All the students are advised to check their NITT WEBMAIL/group mail/suggested by the course faculty, class representative regularly. All the correspondence (schedule of classes/ schedule of assessment/ course material/ any other information regarding this course) will be done through them only.
2. Queries (if required) to the course teacher shall only be emailed to the email id specified by the teacher.

ATTENDANCE

1. Attendance will be taken by the faculty in all the contact hours. Every student should try to be present in the class during these contact hours.

COMPENSATION ASSESSMENT

1. Attending all the assessments are MANDATORY for every student.
2. Every student is expected to score minimum 40% of the maximum mark of the class in the total assessment (1, 2, 3, 4 and 6) to pass the course. Otherwise the student would be declared fail and ‘F’ grade will be awarded. Further he can take up only FORMATIVE ASSESSMENT.
3. Those students who missed any of the continuous assessments (CAs) due to genuine reasons can appear for retest. The scores in the retest will be taken into account for computing marks for CA.

ACADEMIC HONESTY & PLAGIARISM

1. All the students are expected to be genuine during the course work. Taking of information by means of copying simulations, assignments, looking or attempting to look at another student’s paper or bringing and using study material in any form for copying during any assessments is considered dishonest.
2. Tendering of information such as giving one’s program, simulation work, assignments to another student to use or copy is also considered dishonest.
3. Preventing or hampering other students from pursuing their academic activities is also considered as academic dishonesty.
4. Any evidence of such academic dishonesty will result in the loss of marks on that assessment. Additionally, the names of those students so penalized will be reported to the class committee chairperson and HoD of the concerned department.
5. Students who honestly producing ORIGINAL and OUTSTANDING WORK will be REWARDED.

ADDITIONAL INFORMATION

Queries and feedback may also be emailed to the Course Faculty at rkkavitha@nitt.edu
FOR APPROVAL
Course Faculty ____________ **CC-Chairperson** Dr R Malmathanraj **HOD** ____________