NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE PLAN – PART I			
Name of the programme and specialization	B.Tech. Computer Science & Engineering		
Course Title	Computer Organization		
Course Code	CSPC34		
Course Code of Pre-requisite subject(s)	NIL	No. of Credits	3
Session	JULY 2023	Section (if Applicable)	A
Name of Faculty	Dr S. Jaya Nirmala	Department	CSE
Official Email	sjaya@nitt.edu	Telephone No.	
Name of Course Coordinator(s) (if, applicable)	NA		
Official E-mail	-		
Course Type (please tick appropriately)	PC		

Syllabus (approved in BoS)

Refer the Link: https://www.nitt.edu/home/academics/curriculum/B.Tech-CSE-2020.pdf (Page Number 31)

COURSE OBJECTIVES

- To understand the basic hardware and software issues of computer organization
- To understand the representation of data at machine level
- To understand how computations are performed at machine level
- To understand the memory hierarchies, cache memories and virtual memories
- To learn the different ways of communication with I/O devices

MAPPING OF COs with POs

Course Outcomes	Programme Outcomes (PO)
Analyze the abstraction of various components of a computer	3, 7
Analyze the hardware and software issues and the interfacing	3, 5
Work out the trade-offs involved in designing a modern computer system	1, 2, 5, 7, 10, 12
Understand the various memory systems and I/O communication	5, 7

COURSE PLAN – PART II

COURSE OVERVIEW

This course provides an overview of the basic operation of computer hardware and how it interacts with software.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No	Week / Contact Hours	Topic	Mode of Delivery: PPT/ Chalk and Talk
		UNIT I	
1	1	Introduction, Technologies for building Processors and Memory	√
2	2,3	Performance, The Power Wall	√
3	4	Operations of the Computer Hardware	√
4	5	Operands Signed and Unsigned	√
5	6	Representing Instructions	√
6	7,8	Logical Operations	√
7	9	Instructions for Making Decisions	√
		UNIT II	
8	10	MIPS Addressing for 32-Bit Immediate and Addresses	√
9	11,12	Parallelism and Instructions:	√
10	13	Translating and Starting a Program	√
11	14,15	Addition and Subtraction problems	√
12	16	Multiplication Problems	√
13	17	Division Problems	√
14	18	Floating Point Operations and Problems	√
15	19	Parallelism and Computer Arithmetic: Sub word Parallelism	√
16	20	Streaming SIMD Extensions and Advanced Vector Extensions in x86.	√
		UNIT III	
17	21	Logic Design Conventions	√
18	22	Building a Datapath	√

19	23	A Simple Implementation Scheme	√
20	24,25	Overview of Pipelining, Pipelined Datapath, Data Hazards: Forwarding	√
21	26	Control Hazards	√
22	27	Exceptions	√
23	28	Parallelism via Instructions, The ARM Cortex – A8 and Intel Core i7 Pipelines	√
24	29	Instruction–Level Parallelism and Matrix Multiply Hardware Design language	√
UNIT IV			
25	30	Memory Technologies	√
26	31,32	Basics of Caches, Measuring and Improving Cache Performance	√
27	33	Dependable memory hierarchy	√
28	34,35	Virtual Machines, Virtual Memory	√
29	36	Using FSM to Control a Simple Cache	√
30	37	Parallelism and Memory Hierarchy: Redundant Arrays of Inexpensive Disks	√
31	38	Implementing Cache Controllers	√
UNIT V			
32	39	Disk Storage and Dependability	√
33	40	Parallelism and Memory Hierarchy:	√
34	41	Performance of storage systems	√
35	42	Introduction to multi-threading clusters	√
36	43	Message passing multiprocessors	√

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Cycle Test – 1	As per the academic	1 Hour	15
2	Cycle Test – 2	As per the academic	1 Hour	15
3	Assignment 1 and 2	7th and 11th week	NA	10
4	Class tests	-	NA	10
CPA	Compensation Assessment*	As per the academic schedule	1 Hour	15

4	Final Assessment *	As per the academic schedule	3 Hours	50

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

Feedbacks are collected before final examination through MIS or any other standard format followed by the institute.

COURSE POLICY (including compensation assessment to be specified)

MODE OF CORRESPONDENCE (email/ phone etc)

Email: sjaya@nitt.edu

COMPENSATION ASSESSMENT

One Retest will be conducted for absentees in Cycle Tests, for genuine reasons

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- At least 75% attendance in each course is mandatory.
- A maximum of 10% shall be allowed under On Duty (OD) category.
- Students with less than 75% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

ACADEMIC DISHONESTY & PLAGIARISM

- Possessing a mobile phone, carrying bits of paper, talking to other students, or copying from others during an assessment will be treated as a punishable offence.
- Zero marks are to be awarded to the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson, HoD and other members, shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.
- The above policy against academic dishonesty shall be applicable to all the programmes.

ADDITIONAL INFORMATION, IF ANY

The Course Coordinator is available for consultation during official timings

FOR APPROVAL

Course Faculty _____ **CC- Chairperson** _____ **HOD** _____