NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE PLAN – PART I			
Course Title	Advanced Digital Design		
Course Code	CS636	**No. of Credits**	3
Course Code of Prerequisite subject(s)	–		
Session	Jan. 2023	**Section (if, applicable)**	NA
Name of Faculty	Prof. N. Ramasubramanian	**Department**	CSE
Email	nrs@nitt.edu	**Telephone No.**	0431-2503204
Name of Course Coordinator(s) (if, applicable)	NA		
E-mail	NA	**Telephone No.**	NA
Course Type	Elective course		

Syllabus (approved in BoS)

Unit – I Review of Combinational and Sequential logic design – Structural models of combinational logic – Propagation delay – Behavioral Modeling – Boolean equation based behavioral models of combinational logic – Cyclic behavioral model of flip-flop and latches – A comparison of styles for behavioral modeling – Design documentation with functions and tasks

Unit – II Synthesis of Combinational and Sequential logic – Introduction to synthesis – Synthesis of combinational logic – Synthesis of sequential logic with latches – Synthesis of three-state devices and bus interfaces – Synthesis of sequential logic with flip-flops – Registered logic – State encoding – Synthesis of gated clocks and clock enables – Anticipating the results of synthesis – Resets – Synthesis of loops – Design traps to avoid – Divide and Conquer: partitioning a design.

Unit – III Design and Synthesis of Datapath Controllers – Partitioned sequential machines – Design example: Binary counter – Design and synthesis of a RISC stored-program machine – Processor, ALU, Controller, Instruction Set, Controller Design and Program Execution – UART – Operation, Transmitter, Receiver.

Unit – IV Programmable logic devices – Storage devices – Programmable Logic Array (PLA) – Programmable Array Logic (PAL) – Programmability of PLDs – Complex PLDs – Introduction to Altera and Xilinx FPGAs – Algorithms – Nested loop programs and data flow graphs – Design Example of Pipelined Adder, Pipelined FIR Filter – Circular buffers – FIFOs and Synchronization across clock domains – Functional units for addition, subtraction, multiplication and division – Multiplication of signed binary numbers and fractions.

Unit – V Postsynthesis Design Validation – Postsynthesis Timing Verification – Elimination of ASIC Timing Violations – False Paths – Dynamically Sensitized Paths – System Tasks for Timing Verificaion – Fault Simulation and Testing – Fault Simulation – Fault Simulation with Verifault.

COURSE OBJECTIVES

- To understand the basic building blocks, logic gates, adders, multipliers, shifters and other digital devices
- To apply logic minimization techniques, including Karnaugh Maps
- To learn techniques and tools for programmable logic design

COURSE OUTCOMES (CO)

Course Outcomes	**Aligned Programme Outcomes (PO)**
1. Students understand the use standard digital memory devices as components in complex subsystems	PO2, PO6
2. Acquire skill set to develop the necessary software for basic digital systems	PO5, PO6
3. Technical knowhow to design simple combinational logic circuits and logic controllers	PO3, PO4, PO7

COURSE PLAN – PART II

COURSE OVERVIEW

Design and analysis of digital circuit using building blocks, timing in combinational and sequential circuits, programmable logic devices and RISC processor with arithmetic logic units, UART etc.
An introduction to hardware description languages (HDL) such as Verilog and logic synthesis tools, which helps to develop the technical skills to design, simulate, analyze and verify complex digital circuits.

COURSE TEACHING AND LEARNING ACTIVITIES			
S.No.	**Week/Contact Hours**	**Topic**	**Mode of**
1	1/3	Review of Combinational logic design	Chalk & Board
2		Review of Sequential logic design	Power Point
3		Discussion on applications of Combinational and sequential Circuits	Power Point
4	2/3	Structural models of combinational logic Propagation delay	Chalk & Board
5		Behavioral Modeling Boolean equation based behavioral models of combinational logic	Chalk & Board
6		Cyclic behavioral model of flip-flop and latches	Power Point
7	3/3	A comparison of styles for behavioral modeling	Chalk & Board
8		Design documentation with functions and tasks	Power Point
9		Synthesis of Combinational and Sequential logic – Introduction to synthesis	Chalk & Board
10	4/3	Synthesis of combinational logic	Chalk & Board
11		Synthesis of sequential logic with latches and three-state devices and bus interfaces	Chalk & Board
12		Synthesis of sequential logic with flip-flops ,Registered logic and State encoding	Power Point
13	5/3	Synthesis of gated clocks and clock enables and Anticipating the results of synthesis along with Resets	Chalk & Board
14		Synthesis of loops	Chalk & Board
15		Design traps to avoid and Divide and Conquer : partitioning a design.	Power Point
16	6/3	Design and Synthesis of Datapath Controllers	Power Point
17	6/3	Partitioned sequential machines and Design Example: Binary counter	Power Point
18		Design and synthesis of a RISC stored program machine for Processor, ALU, Controller,	Power Point

19	7/3	Instruction Set, Controller Design and Program Execution	Power Point
20		Design Example UART –Operation, Transmitter, Receiver.	Power Point
21		Programmable logic devices – Storage devices	Power Point
22	8/3	Programmable Logic Array (PLA) , Programmable Array Logic (PAL) ,	Power Point
23		Programmability of PLDs and Complex PLDs	Power Point
24		Introduction to Altera and Xilinx FPGAs	Power Point
25	9/3	Discussion on Xilinx FPGAs in more detail	Power Point
26		Algorithms , Nested loop programs and data flow graphs - Introduction	Power Point
27		Algorithms , Nested loop programs and data flow graphs with Examples	Power Point
28	10/3	Design Example of Pipelined Adder and Pipelined FIR Filter	Power Point
29		Circular buffers and FIFOs and Synchronization across clock domains	Power Point
30		Functional units for addition, subtraction, multiplication and division	Power Point
31	11/3	Multiplication of signed binary numbers and fractions	Power Point
32		Postsynthesis Design Validatio and Postsynthesis Timing Verification	Power Point
33		Elimination of ASIC Timing Violations ,False Paths and Dynamically Sensitized Paths	Power Point
34	12/3	System Tasks for Timing Verificaion	Power Point
35		Fault Simulation and Testing – Fault Simulation	Power Point
36		Fault Simulation with Verifault- XL	Power Point
37	13/3	Lab exercises using Vivado	Computer
38			Computer
39			Computer
40	14/3		Computer

COURSE ASSESSMENT METHODS-THEORY (shall range from 4 to 6)				
S. No.	Mode of Assessment	Week/Date	Duration	Marks % Weightage
1.	Cycle Test-1	As per the Academic Schedule	1 hour	15
2.	Cycle Test-2	As per the Academic Schedule	1 hour	15
3.	Quiz	-	-	10
4.	Assignment	1 week before final assessment	-	20
	Compensation Assessment*	As per the Academic Schedule	1 hour	15
5.	End Semester Examination	As per Academic Schedule	3 hours	40
Total				100

*guidelines are provided at next page for Compensation Assessment.

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

1. Students' feedback through class committee meetings.
2. Feedback questionnaire from students – from MIS at the end of the semester.

COURSE POLICY (preferred mode of correspondence with students, compensation assessment policy to be specified)

MODE OF CORRESPONDENCE (email/ phone etc)

Mode of Correspondence through email or Phone.

*** COMPENSATION ASSESSMENT POLICY**

In case of emergency, the student should submit compensatory assignments on submission of appropriate documents as proof. Compensatory assessments would be framed according to the time frame available, and the assessment task missed by the students.

ATTENDANCE POLICY (A uniform attendance policy as specified below shall be followed)

- At least 75% attendance in each course is mandatory.
- A maximum of 10% shall be allowed under On Duty (OD) category.
- Students with less than 65% of attendance shall be prevented from writing the final assessment and shall be awarded 'V' grade.

ACADEMIC DISHONESTY & PLAGIARISM

- Carrying bits of paper, talking to other students, copying from others during an assessment will be treated as punishable dishonesty.
- Zero mark to be awarded for the offenders. For copying from another student, both students get the same penalty of zero mark.
- The departmental disciplinary committee including the course faculty member, PAC chairperson and the HoD, as members shall verify the facts of the malpractice and award the punishment if the student is found guilty. The report shall be submitted to the Academic office.
- The above policy against academic dishonesty shall be applicable for all the programmers.

ADDITIONAL INFORMATION

The students can get their doubts clarified at any time with their faculty member.

FOR APPROVAL

Course Faculty	CC- Chairperson	HOD
(Prof. N. Ramasubramanian)	(Prof. N. Ramasubramanian)	(Dr. S. Mary Saira Bhanu)