DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, TIRUCHIRAPPALLI

COURSE PLAN – PART I			
Course Title	**DIGITAL SYSTEMS DESIGN**		
Course Code	CSPC33	**No. of Credits**	3
Course Code of Pre-requisite subject(s)	Nil		
Session	B.Tech. – CSE	**Section (if, applicable)**	B section
Name of Faculty	B. Shameedha Begum	**Department**	CSE
Email	shameedha@nitt.edu	**Telephone No.**	0431-2503215
Name of Course Coordinator(s) (if, applicable)	NA		
E-mail	NA	**Telephone No.**	NA
Course Type	July – November 2022 Session (Odd Semester)		

Syllabus (approved in BoS)

Unit – I

Binary codes - Weighted and non-weighted - Binary arithmetic conversion algorithms, Canonicaland standard boolean expressions - Truth tables, K-map reduction - Don't care conditions - Adders / Subtractors - Carry look-ahead adder - Code conversion algorithms - Design of code converters - Equivalence functions.

Unit – II

Binary/Decimal Parallel Adder/Subtractor for signed numbers - Magnitude comparator - Decoders / Encoders - Multiplexers / Demultiplexers - Boolean function implementation using multiplexers.

Unit – III

Sequential logic - Basic latch - Flip-flops (SR, D, JK, T and Master-Slave) - Triggering of flip-flops - Counters - Design procedure - Ripple counters - BCD and Binary - Synchronous counters, Registers - Shift registers - Registers with parallel load, Reduction of state and flow tables - Race-free state assignment - Hazards.

Unit – IV

Introduction to VLSI design - Basic gate design - Digital VLSI design - Design of general boolean circuits using CMOS gates. Verilog Concepts – Basic concepts – Modules & ports & Functions – useful modeling techniques – Timing and delays user defined primitives. Modeling Techniques

Unit – V

Advanced Verilog Concepts – Synthesis concepts – Inferring latches and flip-flops –Modeling techniques for efficient circuit design. Design of high-speed arithmetic circuits Parallelism Pipelined Wallace tree tipliers - Systolic algorithms - Systolic matrix multiplication.

Text Book

- Morris Mano and Michael D. Ciletti, "Digital Design", 5th edition, Prentice Hall of India,2012
- Samir Palnitkar, "Verilog HDL", 2nd Edition, Pearson Education, 2003

Reference Books

- Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL, 2nd Edition, Pearson Education, 2010
- Stephen Brown, "Fundamentals of Digital Logic with Verilog", McGraw Hill, 2007

COURSE OBJECTIVES

- To understand the essential knowledge on the fundamentals and applications of digital circuits and digital computing principles.
- To understand the overview on the design principles of digital computing systems.
- To complete a significant VLSI design project having a set of objective criteria and design constraints.

COURSE OUTCOMES (CO)

Course Outcomes	Aligned Programme Outcomes (PO)
Ability to understand the functions of various hardware components and their building blocks.	PO1
Ability to understand the Boolean algebraic expressions to digital design.	PO1, PO6
Ability to design and implement complicated digital systems using Verilog.	PO8

COURSE PLAN – PART II

COURSE OVERVIEW

This course has two main goals: (1) to teach students how a digital computer works and (2) to introduce students to Verilog programming. The hardware component of the course begins by introducing the basic switching components of all digital circuits. It shows how to analyze circuits and also how to build circuits that conform to specified computational properties. It introduces many standard circuits used by all computers, such as logic and shift circuits, arithmetic circuits, and memory circuits. The software part of this course explores the design aspects involved in the realization of CMOS integrated circuits/systems from device up to the register/subsystem level. It addresses major design methodologies with emphasis placed on structured full custom design. The course includes the study of CMOS device. critical interconnect and gate characteristics that determine the performance of VLSI circuits. This course will held the students to earn basic digital VLSI design paradigms and the necessary Verilog HDL constructs that would help them to build combinational and sequential logic circuits in CMOS.

COURSE TEACHING AND LEARNING ACTIVITIES

S.No.	Week/Contact Hours	Topic	Mode of
1	1/1	Binary codes - Weighted and non-weighted	Chalk and talk
2	1/1	Binary arithmetic conversion algorithm	Chalk and talk
3	1/1	Canonicaland standard boolean expressions	Chalk and talk
4	2/1	Truth tables, K-map reduction	Chalk and talk
5	2/1	Don't care conditions	Chalk and talk

6	2/1	Adders	Chalk and talk
7	3/1	Subtractors	Chalk and talk
8	3/1	Carry look-ahead adder	Chalk and talk
9	3 /1	Code conversion algorithms - Design of code converters	Chalk and talk
10	4/1	Binary/Decimal Parallel Adder/	Chalk and talk
11	4/1	Binary/Decimal Parallel Subtractor	Chalk and talk
12	4/1	Magnitude comparator	Chalk and talk
13	5/1	Decoders / Encoders	Chalk and talk
14	5/1	Demultiplexers	Chalk and talk
15	5/1	Multiplexers, Boolean function implementation using multiplexers	Chalk and talk
16	6/1	Sequential logic - Basic latch	Chalk and talk
17	6/1	Flip-flops (SR, D, JK, T and Master-Slave)	Chalk and talk
18	6/1	Counters - Design procedure	Chalk and talk
19	7/1	Ripple counters - BCD Counters	Chalk and talk
20	7/1	Binary - Synchronous counters,	Chalk and talk
21	7/1	Registers - Shift registers	Chalk and talk
22	8/1	Reduction of state and flow tables	Chalk and talk
23	8/1	Race-free state assignment - Hazards	Chalk and talk
24	8/1	Introduction to VLSI design - Basic gate design	Chalk and talk
25	9/1	Verilog Concepts – Basic concepts	Chalk and talk
26	9/1	Modules & ports & Functions	Chalk and talk
27	9/1	Useful modeling techniques	Chalk and talk
28	10/1	Timing and delays–user defined primitives	Chalk and talk
29	10/1	Advanced Verilog Concepts – Synthesis	Chalk and talk
30	10/1	Inferring latches and flip-flops	Chalk and talk
31	11/1	Modeling techniques for efficient circuit design	Chalk and talk
32	11/1	Design of high-speed arithmetic circuits	Chalk and talk
33	11/1	Parallelism Pipelined Wallace tree tipliers	Chalk and talk

34	12/1	Systolic algorithms - Systolic matrix multiplication	Chalk and talk
35	12/1	Tutorial	Chalk and talk

COURSE ASSESSMENT METHODS (shall range from 4 to 6)

S.No.	Mode of Assessment	Week/Date	Duration	% Weightage
1	Cycle test 1	As per Schedule	1 Hr	20
2	Cycle test 2	As per Schedule	1 Hr	20
3	Assignment	1 week before final assessment	1 week	10
CPA	Compensation assessment	As per Schedule	1 Hr	20
4	Final Assessment *	As per Schedule	3 Hrs	50

***mandatory; refer to guidelines on page 4**

COURSE EXIT SURVEY (mention the ways in which the feedback about the course shall be assessed)

1. Online feedback
2. Live feedback in the class

COURSE POLICY (preferred mode of correspondence with students, policy on attendance, compensation assessment, , academic honesty and plagiarism etc.)

MODE OF CORRESPONDENCE (email/ phone etc)

Email correspondence is preferable

ATTENDANCE

75% Attendance is mandatory. Students need to commit about their attendance plan within first two weeks.

COMPENSATION ASSESSMENT

To be absent from cycle test 1 & 2 prior permission from the faculty is required.

ACADEMIC HONESTY & PLAGIARISM

- Students should attend the classes sincerely and maintain discipline
- Students should not do any kind of malpractice like copying etc., with regard to the writing of cycle tests and assignments.

ADDITIONAL INFORMATION

Students can contact the faculty to clarify their doubts in person any time during working hours

FOR APPROVAL

Course Faculty	CC-Chairperson	HOD
16/8/22	19/8/2022	19/8/2022