



**Department of Computer Science and Engineering  
National Institute of Technology, Tiruchirappalli**

<b>1. Course Outline</b>			
<b>Course Title</b>	<b>DIGITAL SYSTEMS DESIGN LABORATORY</b>		
<b>Course Code</b>	CSLR32		
<b>Programme, Department &amp; Section</b>	B.Tech. – CSE B section	<b>No. of Credits</b>	3
<b>Co-requisites Course Code</b>	--	<b>Faculty Name</b>	B. Shameedha Begum
<b>E-mail</b>	<a href="mailto:shameedha@nitt.edu">shameedha@nitt.edu</a>	<b>Telephone No.</b>	0431 - 2503215
<b>Course Type</b>	LR		
<b>Session in Academic Year</b>	July – November 2022 Session (Odd Semester)		

<b>2. Course Overview</b>								
- This covers design and implementation of Digital circuits.								
<b>3. Course Objectives</b>								
<ul style="list-style-type: none"> <li>- To develop programs in Hardware Description Language</li> <li>- To design and implement synchronous sequential, asynchronous sequential circuits</li> <li>- To be familiar with basic combinational and sequential components used in the typical data path designs</li> </ul>								
<b>4. Course Outcomes (CO)</b>								
<ul style="list-style-type: none"> <li>- Ability to design synchronous sequential circuits using basic flip-flops, counters, PLA, PAL</li> <li>- Ability to design and develop basic digital circuits</li> <li>- Ability to debug digital circuits</li> </ul>								
<b>5. Course Outcomes (CO)</b>	<b>Aligned Programme Outcome (PO)</b>							
	<b>PO-1</b>	<b>PO-2</b>	<b>PO-3</b>	<b>PO-4</b>	<b>PO-5</b>	<b>PO-6</b>	<b>PO-7</b>	<b>PO-8</b>
Ability to design synchronous sequential circuits using basic flip-flops, counters, PLA, PAL.	S	M	S	S	S	S	B	M
Ability to design and develop basic digital circuits	S	S	S	S	S	M	B	M
Ability to debug digital circuits	M	M	S	M	S	M	B	M

S = 0.6

M = 0.4

B = 0.0

## 6. Course Teaching and Learning Activities

S.No	Title	Type		Mode of delivery			
		L	T	C&T	PPT	VL/VC	DEMO
1	Study of Logic Gates	√					
2	Design of Adders						√
3	Design of Subtractors						√
4	Conversion of Binary to Excess-3						√
5	Design of Encoders and Decoders						√
6	Parity Generator and Checker						√
7	Design of a Multiplexor						√
8	Design of a Magnitude Comparator						√
9	Design of a Demultiplexor						√
10	Implementation of T, JK Flip-flops						√
11	Conversion of Flip Flops						√
12	3-Bit Synchronous and Asynchronous Counter						√
13	Design and Implementation of Shift Registers						√
14	HDL Implementation of 4:1 Multiplexor						√
15	HDL Implementation of 4-Bit Full Adder						√
16	HDL Implementation of 4-Bit Ripple Counter						√


## 7. Course Assessment Methods

Sl. No.	Mode of Assessment	Week / Date	Duration	Marks
1	Continuous Assessment	Every Lab Session	3 hours	20
2	Record	Every Lab Session	-	10
3	Model Exam	6 <sup>th</sup> Week	3 hours	45
4	End Semester Exam	As per schedule	3 hours	25
			Total	100

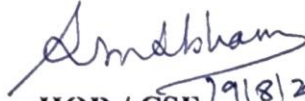
## 8. Essential Readings (Textbooks, Reference books, Websites, Journals, etc.)

1. Morris Mano and Micheal D. Ciletti, "Digital System Design", 5th Edition, PHI, 2012
2. Samir Palnitkar, "Verilog HDL", 2nd Edition, Pearson Education, 2003

### For Senate's Consideration

  
16/8/22  
Course Faculty

  
19/8/2022  
Class Committee Chairperson

  
7/9/8/2022  
HOD / CSE