EC833

(12)

Functional Verification using Hardware Verification Languages

Pre-Requisite: Hardware Description Languages

Course Objective:

- To understand the various Testing attributes and develop the test bench for VLSI architectures.
- To know the techniques to test and validate the circuit and also find the critical path using minimal test vectors.
- To enable students to design VLSI system with appropriate testing schemes.
- To encourage students to develop and implementation the various Test fixtures for different optimized hardware.

System Verilog (SV) - Data Types, Arrays, Structures, Unions, Procedural Blocks, Tasks & Functions, Procedural Statements, Interfaces, Basic OOPs, Randomization, Threads & Inter Process Communication, Advanced OOPs & Test bench guidelines, Advanced Interfaces,

A Complete System Verilog Test Bench (SVTB), Functional Coverage in System Verilog, Interfacing with C, FSM Modeling with SV, Connecting Test bench & Design, Behavioral & Transaction Level Modeling with SV

System Verilog Assertions (SVA) – Introduction to SVA, Building blocks, Properties, Boolean expressions, Sequence, Single & Multiple Clock definitions, Implication operators (Overlapping & Non-overlapping), Repeatition operators, Built-in System functions ($past, $stable, $onehot, $onehot0, $isunknown), Constructs (ended, and, intersect, or, first_match, throughout, within, disableiff, expect, matched, if –else), assertion directives, nested implication, formal arguments in property,

SVA using local variables, calling subroutines, SVA for functional coverage, Connecting SVA to the Design or Test bench, SVA for FSMs, Memories, Protocol checkers, SVA Simulation Methodology, Assertions: Practice & Methodology, Re-use of Assertions, Tracking coverage with Assertions, Using SVA with other languages.

Functional Verification coverage using design, verification languages and implementation standards: Verilog IEEE 1364, VHDL IEEE 1076, SystemVerilog IEEE 1800, Property Specific Language (PSL) IEEE 1850, SystemC™ IEEE 1666, Encryption IEEE 1735, *e* Verification Language IEEE 1647, Open Verification Methodology (OVM) and Universal Verification Methodology (UVM).

Course Outcomes:

Students able to

- Understand the various Testing attributes and develop the test bench for various VLSI architectures.
- Understand the techniques to test and validate the circuit and also find the critical path using minimal test vectors.

Senate

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