CSAKO FPGA Programming Techniques No Roers 3 credit.

Programmable logic devices - PLE, PAL and PLAs - SPLD Vs CPLD - Field programmable logic arrays -techniques to program: one-time programmable, insystem programmable techniques.

UNIT 2

VHDL- Modeling styles - Dataflow - Behavioral - structural designs - Design of simple / complex combinational circuits – sequential circuit design with clocking schemes.

UNIT 3

Verilog HDL - Modeling styles - Dataflow - Behavioral - structural designs compiler directives - operands - operators - gate level modeling - user defined primitives – system tasks and functions – verification using test bench – waveform generation.

UNIT 4

Embedded C programming concepts - architectural design - editing - compiling linking - loading debugging programs - Introduction to C-to-Hardware Compilation Technology - Design of custom FPGA logic using C.

UNIT 5

Capture of the Design - Targeting the Design to the FPGA Device - Processing the Design - Using the Accumulator - Accelerating processing systems -Communication establishment using Ethernet port in FPGA – programs related to communication ports.

References:

- 1. J. Bhasker, "A VHDL primer", 3rd edition, Pearson Education, 2015.
- 2. J. Bhasker, "A Verilog HDL primer", BS publications, 2008.
- 3. David Pellerin, "Practical FPGA Programming in C", Prentice Hall, 2005 of FOOT