CS685 Cache Coherence for Multi-core Architectures

Objectives

- To explore basics of cache memory
- To shed light on the basics of large cache design
- To provide an in-depth knowledge in different cache coherence techniques
- To provide knowledge about different cache simulators

Unit I : Basics of Cache Memory and Cache Design

Basics of Caches, Measuring and Improving Cache Performance, Virtual Memory, A Common Framework for Memory Hierarchies, Cache Memory Principles, Elements of Cache Design

Large Cache Design: Shared vs. Private Caches, Centralized vs. Distributed Shared Caches, Uniform Cache Access, Non-Uniform Cache Access, D-NUCA, S-NUCA, Inclusion, Exclusion, Difference between transaction and transactional memory, STM, HTM

Unit II : Consistency Models and Cache Coherence

Introduction to Consistency and Coherence, Coherence Basics, Cosistency Models: Memory Consistency Motivation and Sequential Consistency, Relaxed Memory Consistency, Weak consistemcy

Unit III : Coherence Protocols

Overview of coherence protocol design space, Coherence Protocols – Snoopy coherence protocols: MSI, MESI, MOESI, Non-Atomic Bus, Case Study IBM Power5; Directory coherence Protocols: Adding exclusive and owned states, Representing directory state, Directory organizations, Performance and scalability optimizations, Case Study Intel QPI

Unit IV : Advanced Topics in Coherence

System Models: Instruction caches, TLBs, Virtual Caches, Write-Through Caches, Coherent DMA, Multilevel Caches and Hierarchical Coherence Protocols; Performance optimizations: Migratory sharing and False sharing optimizations; Maintaining Liveness: Deadlock, Livelock, Starvation; Token Coherence

Unit V : Common Performance Metrics and Study of Cache Simulators

Common Performance Metrics addressed in Cache Coherence, Study of CACTI and GEM 5 Simulators

Text Books:

1. Computer Organization and Design , John L. Hennessy, David A. Patterson , Third Edition, 2005, *Morgan Kaufmann Publisher.*
2. Computer Organization and Architecture, William Stallings, Eighth Edition, 2010, *Prentice Hall*
3. Multi-Core Cache Hierarchies, Rajeev Balasubramonian, Norman P. Jouppi, Naveen Muralimanohar, 2011, *Morgan & Claypool.*
4. Memory Systems: Cache, DRAM, Disks, Bruce Jacob, Spencer W. NG, David T. Wang, *Morgan Kaufman Publisher.*
5. A Primer on Memory Consistency and Cache Coherence, Daniel J. Sorin, Mark D. Hill, and David A. Wood , 2011, *Morgan & Claypool.*