

## Annexure - III

### EMBEDDED MULTICORE SYSTEMS

#### UNIT 1:

Multi-core Architectures- Multicore architecture drivers-Basic multicore hardware architecture overview-Specific multicore architecture characteristics-Processing architectures-ALU processing architectures-Lightweight processing architectures-Mediumweight processing architectures Heavyweight processing architectures-Communication architectures-Memory architectures Application specificity-Application-specific platform topologies-Integration of multicore systems, MPSoCs and sub-systems

#### UNIT 2:

Memory Models for Embedded Multicore Architecture-Memory types-Memory architecture-Cache -Cache customization-Special-purpose memory-Memory structure of multicore architecture-Shared memory architecture-Uniform memory access (UMA)-Non-uniform memory access (NUMA) Distributed memory architecture-Cache coherency-Transactional memory

#### UNIT 3:

Design Considerations for Multicore SoC Interconnections-Transaction-based communication- Storage-oriented transactions-Concurrency of communication and segregation of traffic-Recent trends in SoCs-Functional requirements and topologies of SoC traffic-Memory organization- Implications of inter-device communication paradigms-performance considerations-Interconnection Networks-Building blocks of scalable interconnections-Evaluating and comparing interconnections strategies

#### UNIT 4:

Partitioning Programs for Multicore Systems-parallelism-A high-level partitioning algorithm -Breaking dependencies-Types of dependencies-Canonical dependencies-Read after write-Write after read-Write after write-Read after read-Ordering dependencies-Compute and memory dependencies-Critical sections-Synchronizing data

#### UNIT 5:

Multicore Synchronization Hardware-Instruction set support for synchronization-Test-and-set Compare-and-swap-Load-reserved/store-conditional-Creating new primitives-Compiler intrinsics- Hardware support for synchronization-Bus locking-Hardware support for lock-free programming Lock-free synchronization with hardware queues-Decorated storage operations-Messaging-Memory subsystem considerations-Bare metal systems-Architectural arrangements-Data parallelism: SIMDFunctional parallelism: pipelines-Multicore debug-Trace methods for multicore debug analysis-Types of instrumentation logic blocks-Debug flows and subsystems

#### TEXT BOOK:

- 1.Real world Multi-Core Embedded Systems by Bryon Moyer, Elsevier Publisher,2013.
- 2.Multi-Core Embedded Systems by Georgios Kornaros, CRC Press,2010 .

Mrs. P.B.  
M  
23/11/2017

Mrs. K.V.L. / Sena  
M  
23/11/2017